Introduction of Fast Electronics

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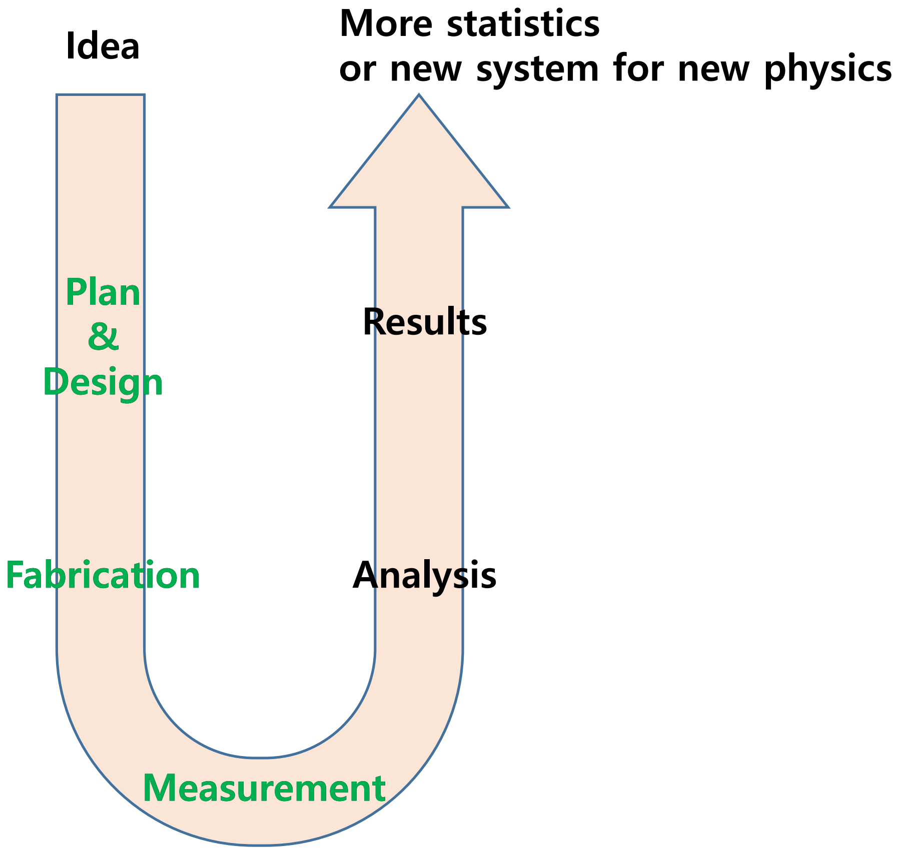
- **Role of DAQ in HEP experiment**
- **Readout scheme for DAQ**
- **Fast electronics**
  - Signal and Device impedance
  - Preamplifier
  - Fan-In and Fan-Out
  - Discriminator (LED & CFD)
  - Logic Unit for coincidence
  - TDC & ADC
- **Summary**

2021. Feb. 15

인하대학교

Role of DAQ System in HEP experiment

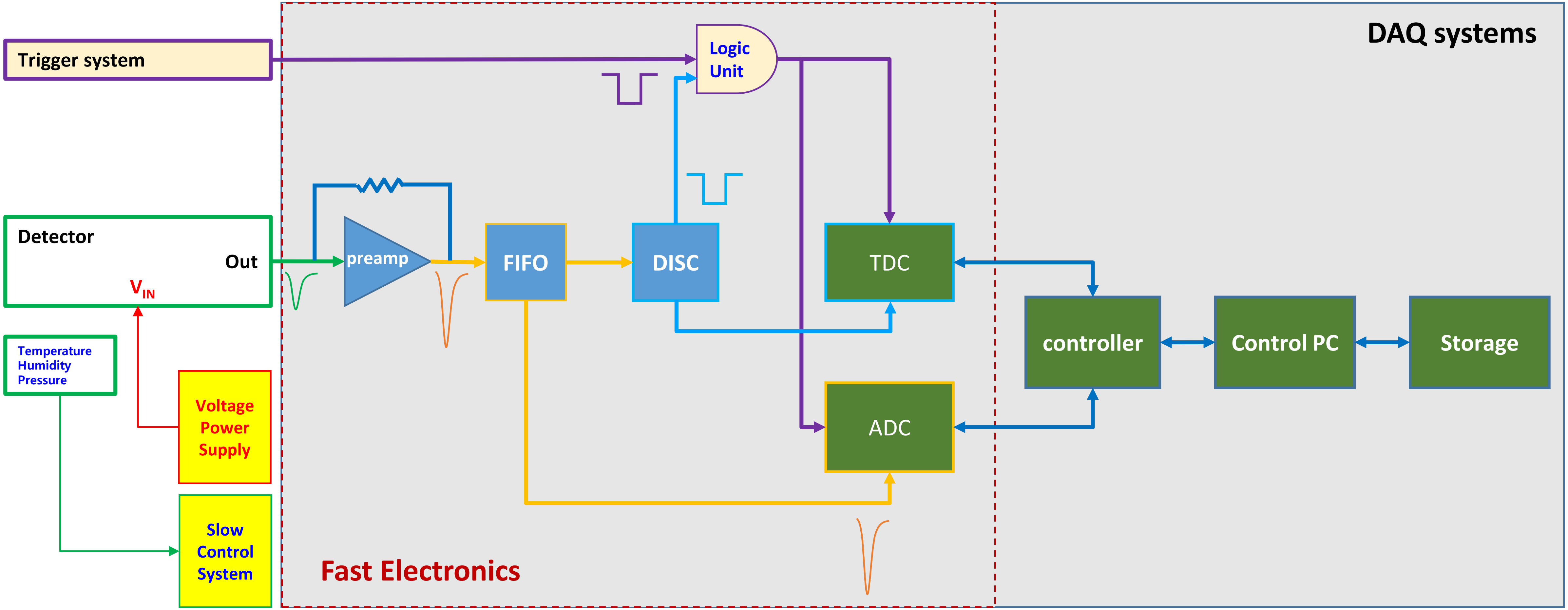
How do we watch an event in HEP experiments?



Five Ws & Hows	Measurement of particle detection
Why	Why needs information about particles ➔ to find out why they are existed and created
	Plan & Design ➔ Fabrication ➔ Measurement
How	How particle interacts with materials
Where	Position where interaction happens
When	Time when interaction happens
Who/Which	Which particles ➔ PID
What	What characteristics of particles

We design, fabricate, test, and use the readout system (or fast electronics) for data acquisition (DAQ).

Readout scheme for data acquisition (DAQ)



Components of waveform

Base line
Pulse height
Pulse width

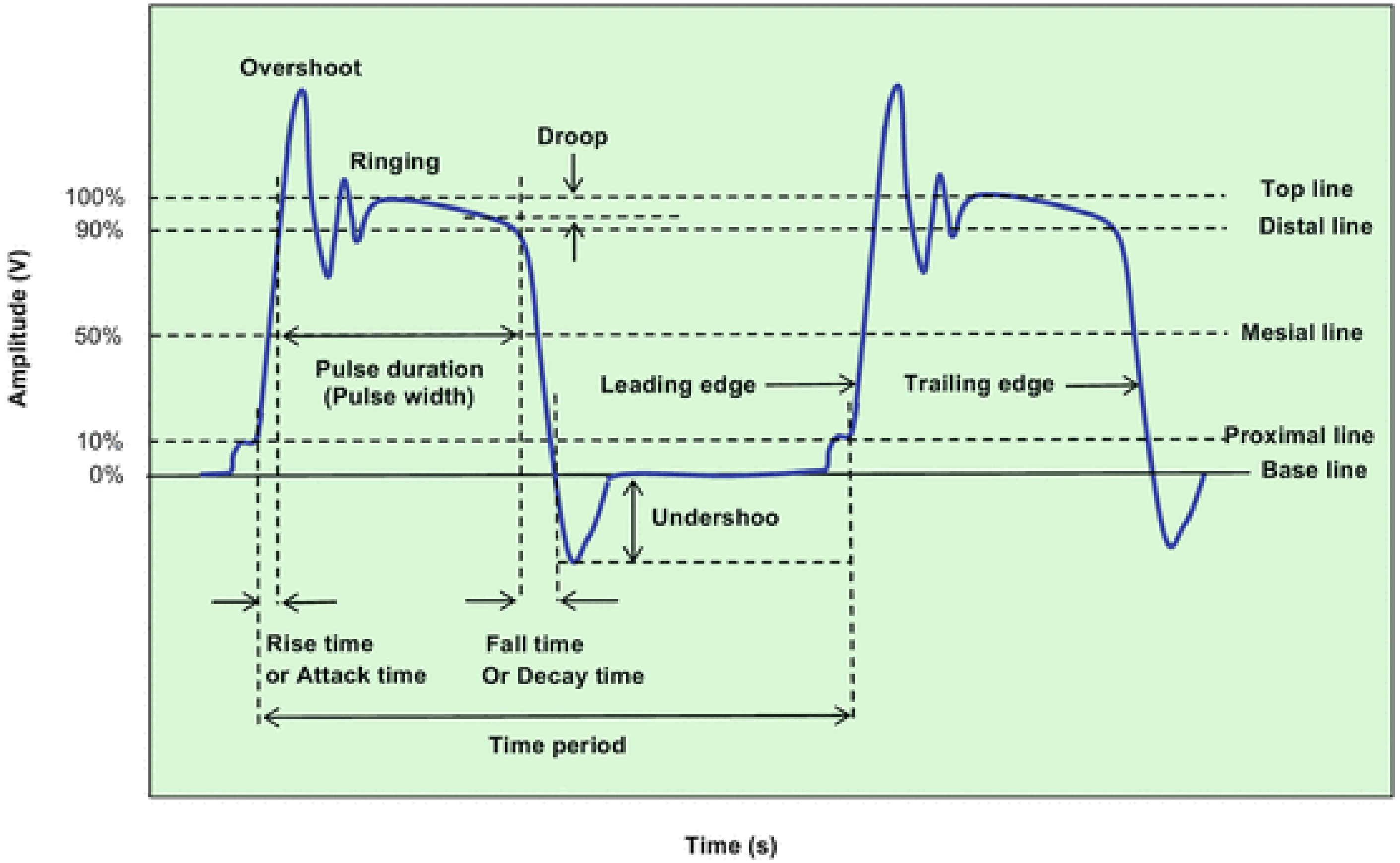
Proximal line: 10% of pulse height
Mesial line: 50% of pulse height
Distal line: 90% of pulse height

Rise time (or attack time) **at leading edge**
Fall time (or decay time) **at trailing edge**
➔ These depend on the polarity of waveform.

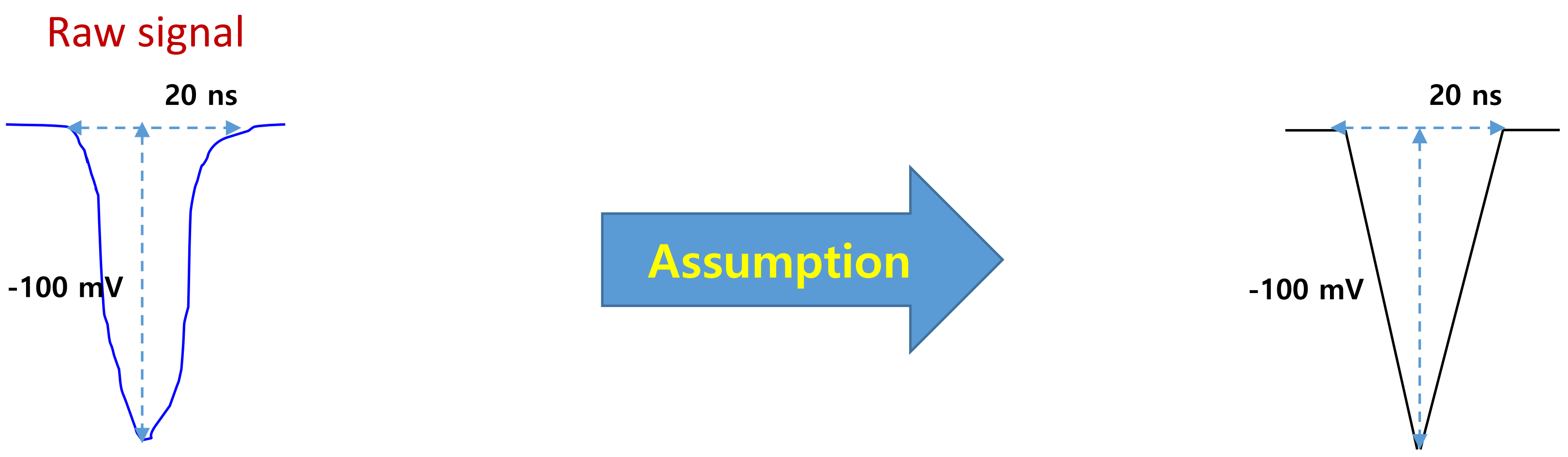
Overshoot
Undershoot
Ringing

Time period

https://link.springer.com/chapter/10.1007/978-3-319-25448-7_7



Charge of raw signal



Electric charge of analog signal with assumption:

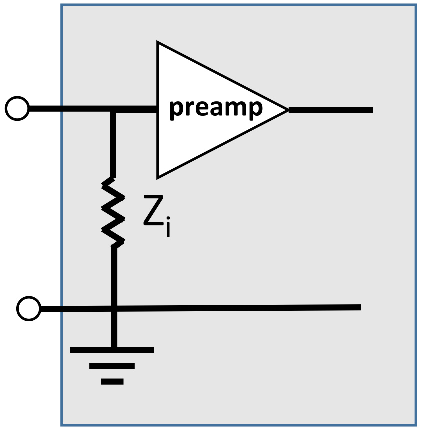
$$Q(C) = \frac{V(V) \cdot t(s)}{2 \cdot R(\Omega)} = \frac{-0.1\,V \cdot 20\,ns}{2 \cdot 50\Omega} = -20\,pC$$

Device impedances

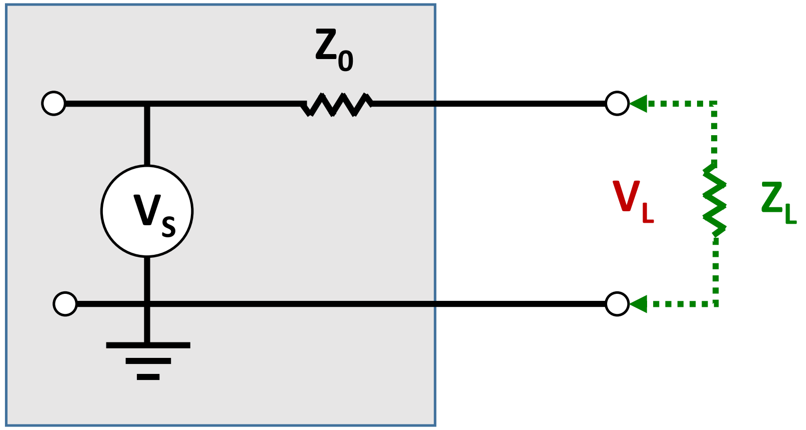
Radiation Detection and Measurement, Glenn F. Knoll

A basic concept in the processing of pulses from radiation detectors is the impedance of the devices that comprise the signal-processing chain.

Input configuration



output configuration



Voltage (V_L) appearing across a loading (Z_L) by voltage-divider relation

$$V_L = V_S \frac{Z_L}{Z_0 + Z_L}$$

For the open-circuit or unloaded ($Z_L = \infty$), voltage is $V_L = V_S$. ➔ not for the real experiment

To preserve maximum signal level, one normally wants V_L to be as large a fraction of V_S as possible.
For $Z_L \gg Z_0$ then $V_L \cong V_S$ ➔ Fan-In & Fan-Out, Discriminator, ADC, etc

For $Z_L = Z_0$ then $V_L = V_S/2$ ➔ Divider or Splitter

Preamplifier

Radiation Detection and Measurement, Glenn F. Knoll
https://www.sciencedirect.com/topics/physics-and-astronomy/preamplifiers

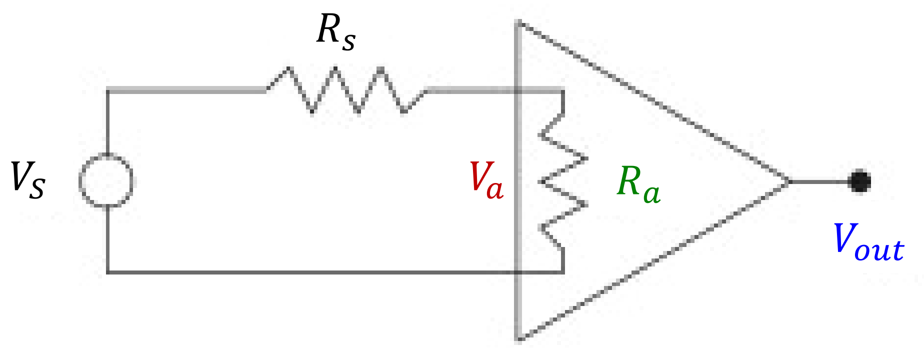
Role	converting a raw signal from the detector into output signal with gain
Location	placing close to the detector to reduce the noise and avoid the signal loss

✓ **Specification for design**
- Dynamic range
- Size of input signal
- Pulse pileup
- Signal-to-noise ratio
- Power consumption

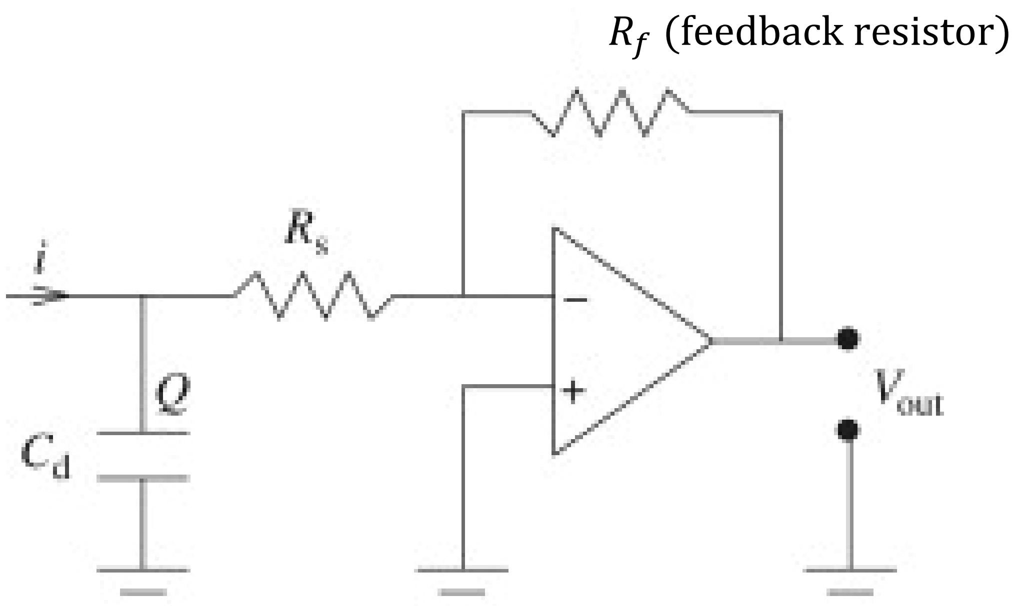
✓ **Configuration**
- Voltage-sensitive preamplifiers
- Current-sensitive preamplifiers
- Charge-sensitive preamplifiers

Voltage-sensitive preamplifiers

https://www.sciencedirect.com/topics/physics-and-astronomy/preamplifiers



Design principle of V-sensitive preamp



Simplified realistic V-sensitive preamp

Signal voltage V_S
Voltage at the input stage of the amplifier V_a
Output voltage V_{out}

$$V_a = V_S \frac{R_a}{R_s + R_a}$$

Any current drawn would decrease the potential drop across $R_{s.}$
Ideally, its input resistance have to be infinite.
But it can only be achieved up to a good approximation.

For $R_a \gg R_S$ then $V_a \cong V_S$
then $V_{out} = Gain \times V_a \approx Gain \times V_S$

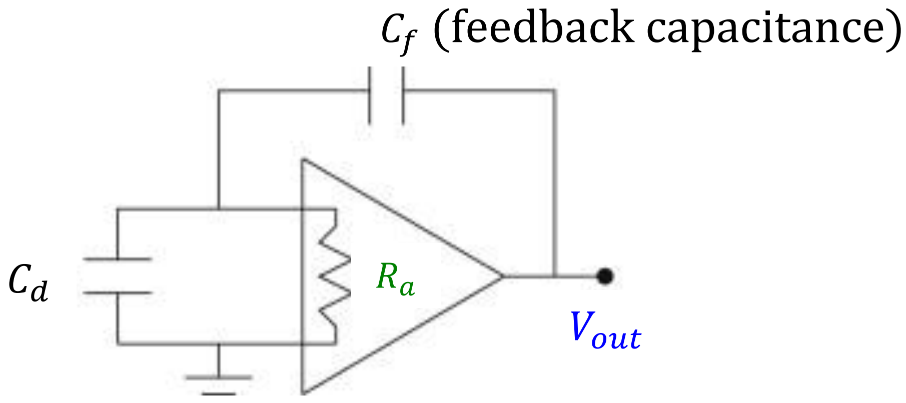
Signal voltage $V_S = Q/C_d$
Q: collected charge on the readout electrode ($Q = \int_0^{t_0} i_s(t)\, dt$)
C_d: combined detector and stray capacitance

then $V_{out} \approx Gain \times \frac{Q}{C_d} = \frac{Gain}{C_d} \int_0^{t_0} i_s(t)\, dt$

Since we are integrating the current to convert it into voltage, **C_d should discharge slower than the charge collection time** $t_d << R_a C_d$.

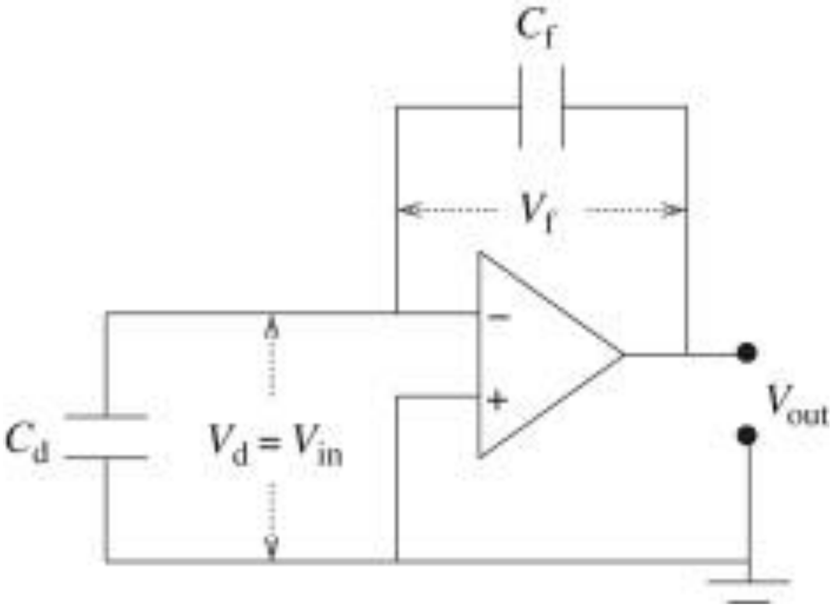
Charge-sensitive preamplifiers

https://www.sciencedirect.com/topics/physics-and-astronomy/preamplifiers



Basic principle of Q-sensitive preamp

The dependence of a voltage-sensitive preamplifier on the input capacitance is a serious problem for many detection systems.
➔ to develop Q-sensitive preamplifiers



Simple Q-sensitive preamp

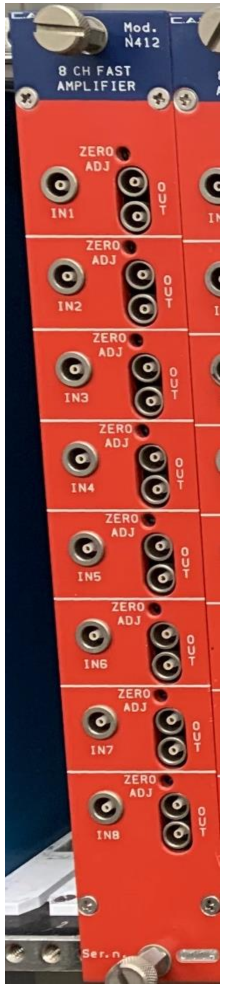
The charge (Q_d) accumulated on the electrode (C_d) is integrated on another capacitor (C_f). Then the potential (V_f) on that capacitor is then directly proportional to the original charge (Q_d) on the detector.

$$V_{out} \propto \frac{Q_f}{C_f} \propto \frac{Q_d}{C_f}$$

The condition that $Q_f \approx Q_d$ can only be achieved if no current flows into the preamplifier's input with $R_a \rightarrow \infty$.

Preamplifiers

https://www.caen.it



CAEN N412 8ch Fast Amplifier

INPUTS:

- 50Ω impedance.
- Reflection coefficient: ≤ 6% over input dynamic range.
- Quiescent voltage: < ± 5 mV.

OUTPUTS:

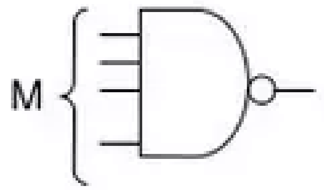
- Risetime: ≤ 3.0 ns.
- Falltime: ≤ 2.0 ns.
- Maximum positive amplitude (linear): 400 mV (50Ω impedance).
- Maximum negative amplitude (linear): -4 V (50Ω impedance).
- Overshoot: ± 10% for input risetimes of 2 ns and with the 2nd output terminated in 50Ω.
- Quiescent voltage adjustable (via front panel trimmer for each channel) in the range from -20 mV to +50 mV.

GENERAL:

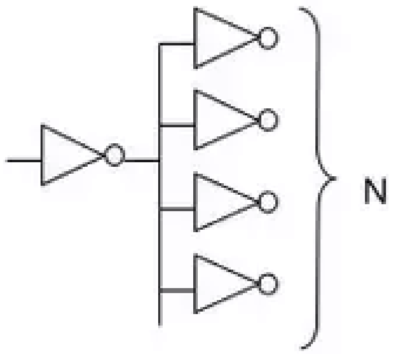
- Gain: fixed 10 ± 3%, non-inverting.
- Coupling: direct.
- I/O delay: ≤ 12 ns.
- Noise: less than 1 mV, referred to input.
- Interchannel crosstalk: better than -56 dB in the worst test condition, and with both the outputs of the tested channel terminated in 50Ω.
- Bandwidth:
  - 160 MHz (with both the channel's outputs terminated in 50Ω);
  - 180 MHz (single ended output).

Fan-In and Fan-Out (FIFO)

Fan-in: maximum number of input signals feeding into the input of a logic system

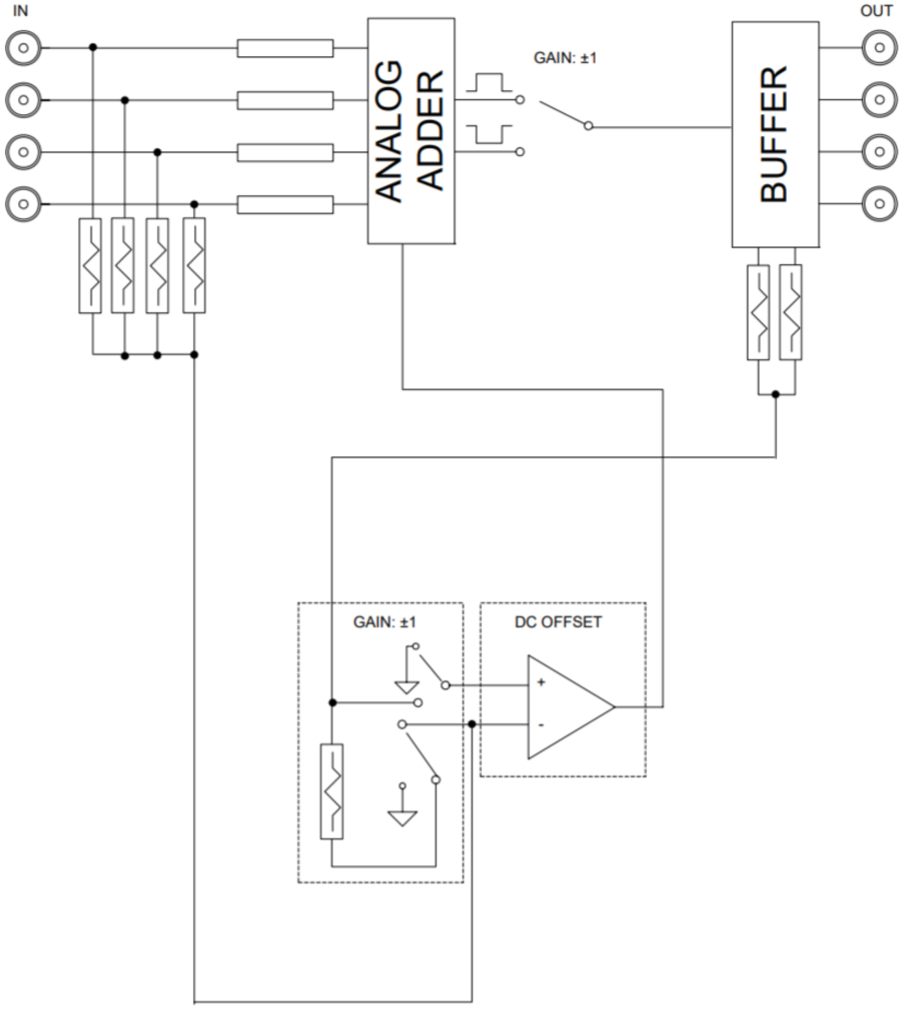


Fan-out: maximum number of output signals from the output of a logic system

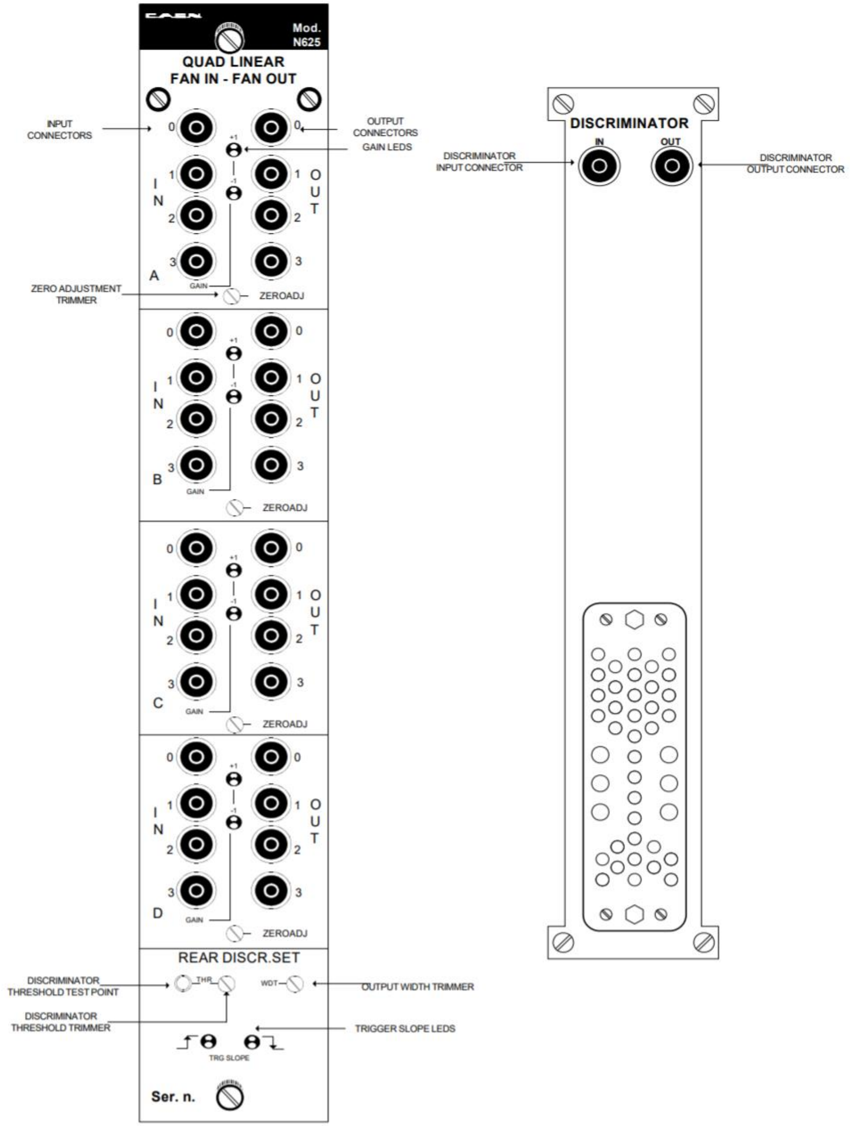


Fan-In and Fan-Out (FIFO)

https://www.caen.it



CAEN N625 Quad Linear Fan In / Fan Out

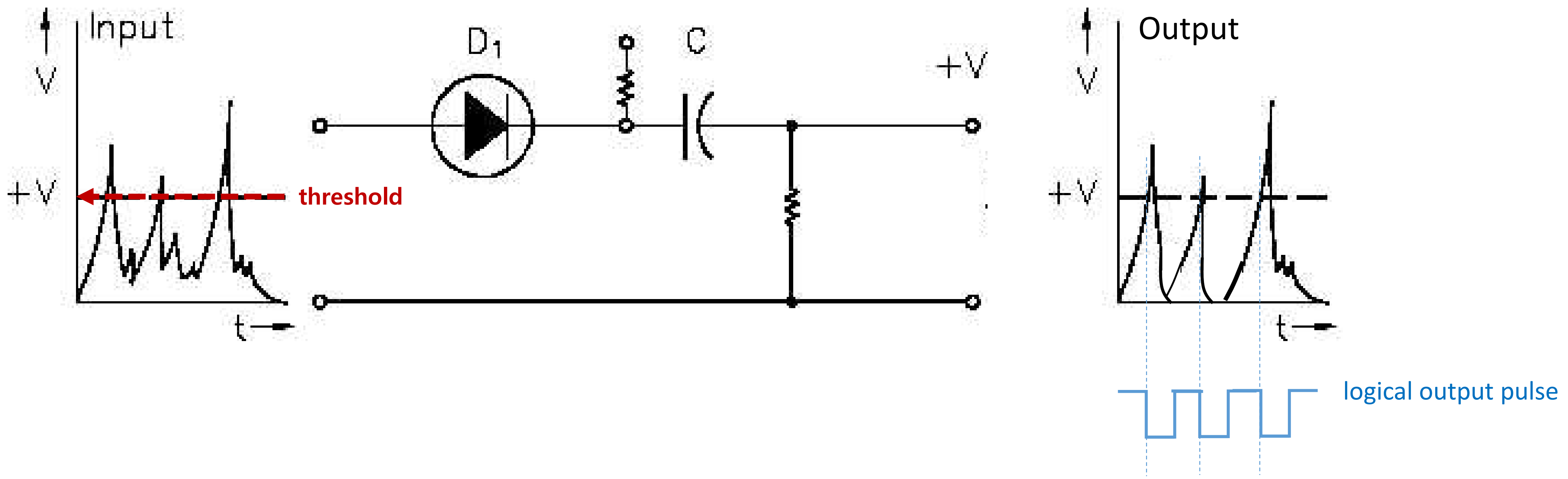


Discriminator (DISC)

http://nuclearpowertraining.tpub.com/h1013v2/css/Discriminator-Circuit-83.htm

Role: generating the logical output pulse when the input pulse exceeds the discriminator preset level

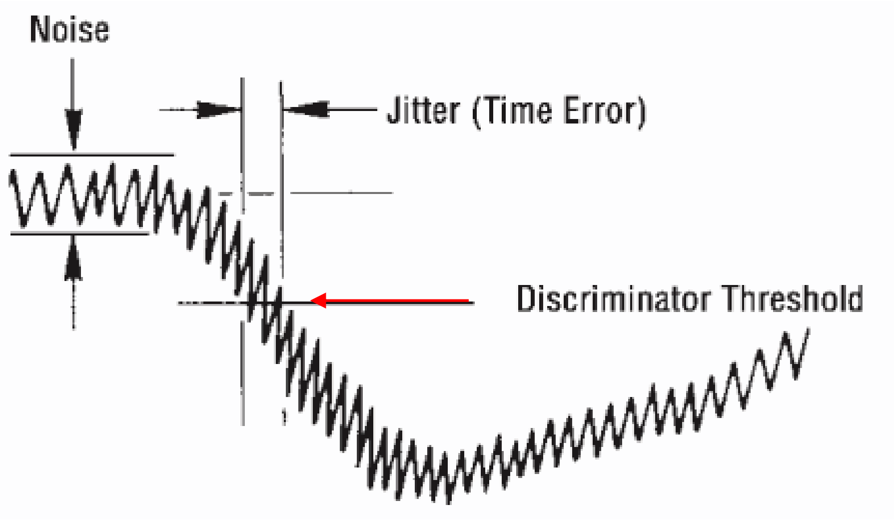
➔ If input voltages **exceeds the threshold value +V** then diode D_1 conducts and **DISC generates the logical output pulses**.



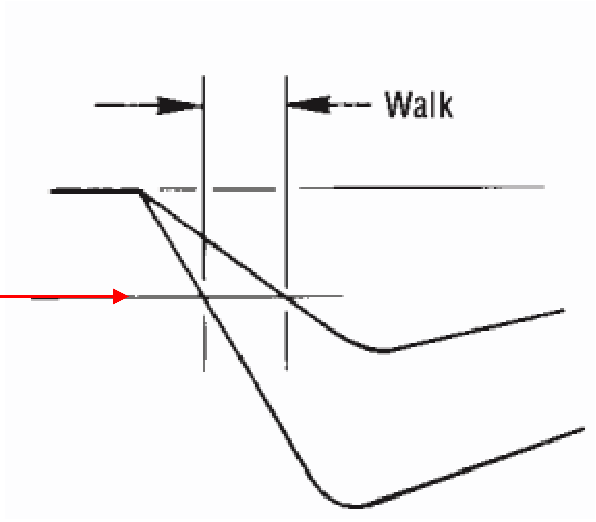
Timing jitter and walk

http://www.peo-radiation-technology.com/wp-content/uploads/2015/09/ort_15_fast-timing-discriminators_datasheet_peo.pdf

Timing jitter in a pulse



Timing walk among pulses



The contribution of noise to the (Timing) Jitter

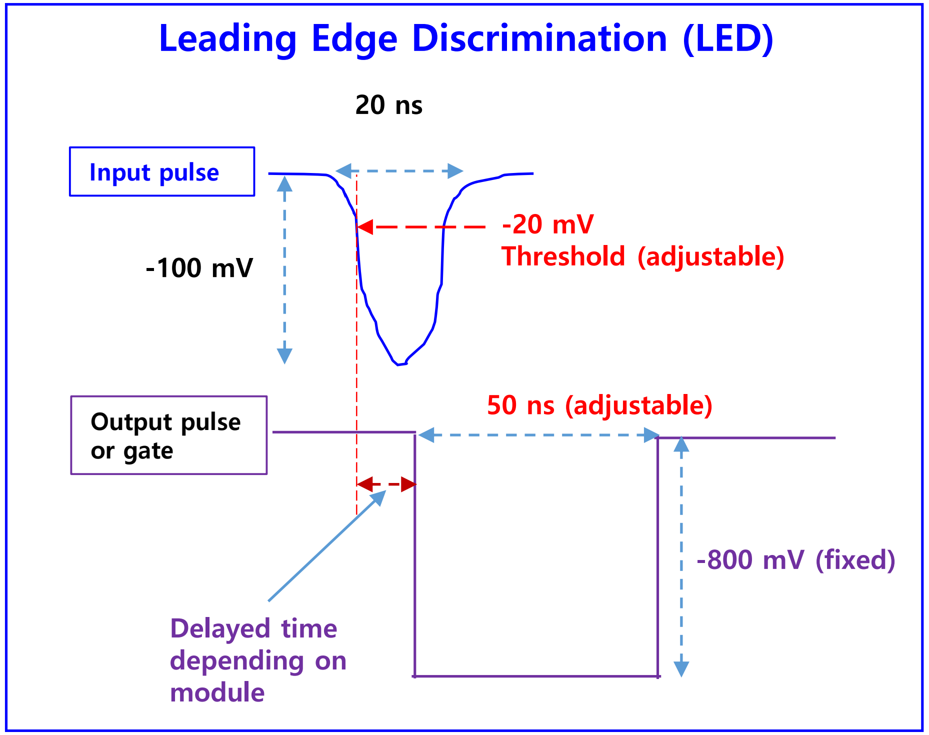
$$\text{Timing Jitter} = e_{noise}/(dV/dt)$$

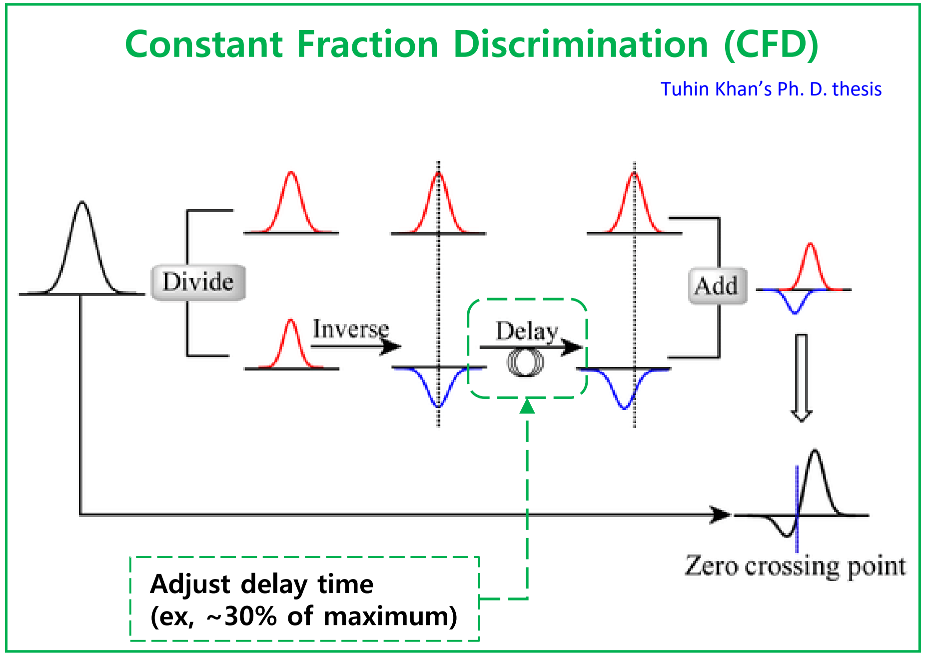
e_{noise}: voltage amplitude of the noise superimposed on the analog pulse

dV/dt: slope of the signal when its leading edge crosses the discriminator threshold

"(Timing) Walk" is the **systematic dependence** of the time marker **on the amplitude of the input pulse.**

LED and CFD





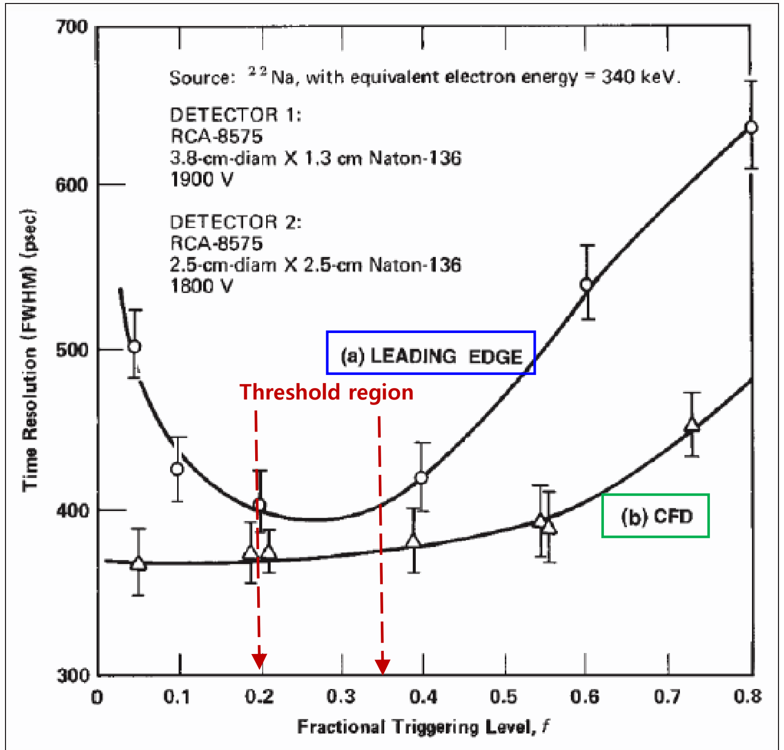


Fig. 2. A Comparison of Leading-Edge Timing with Constant-Fraction Timing for a Narrow Pulse-Height Range. The source was ^{22}Na, with the selected equivalent electron energy in the scintillator = 340 keV. The time resolution (FWHM) is Δ t.

http://www.peo-radiation-technology.com/wp-content/uploads/2015/09/ort_15_fast-timing-discriminators_datasheet_peo.pdf

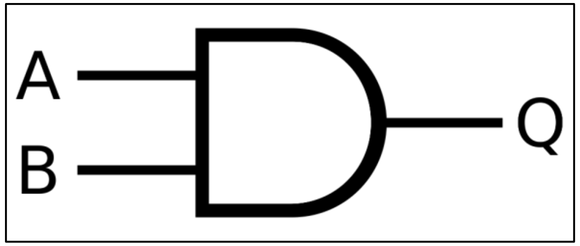
Time resolution: $\sigma_{CFD} < \sigma_{LED}$

Role of Logic Unit

https://www.wekipedia.com

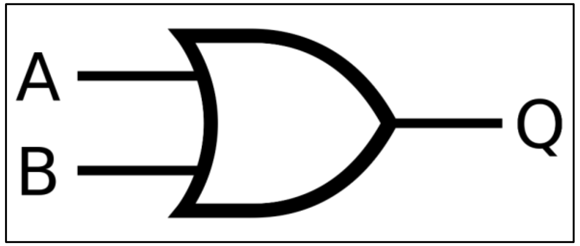
Role: generating the gating pulse when the preset of logical algorism against with inputs is true

AND logic: $A \cdot B$ **or** $A \wedge B$



INPUT		OUTPUT
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

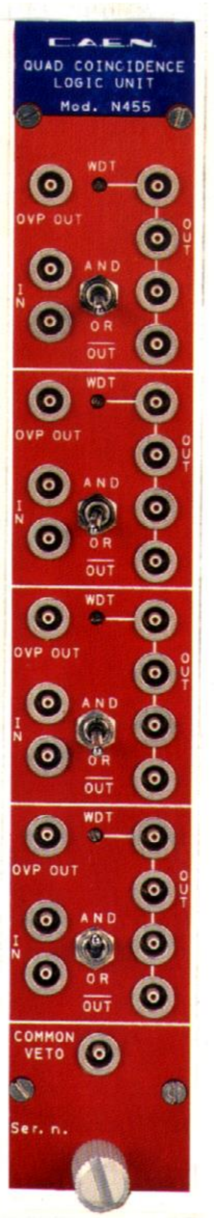
OR logic: $A + B$ **or** $A \vee B$

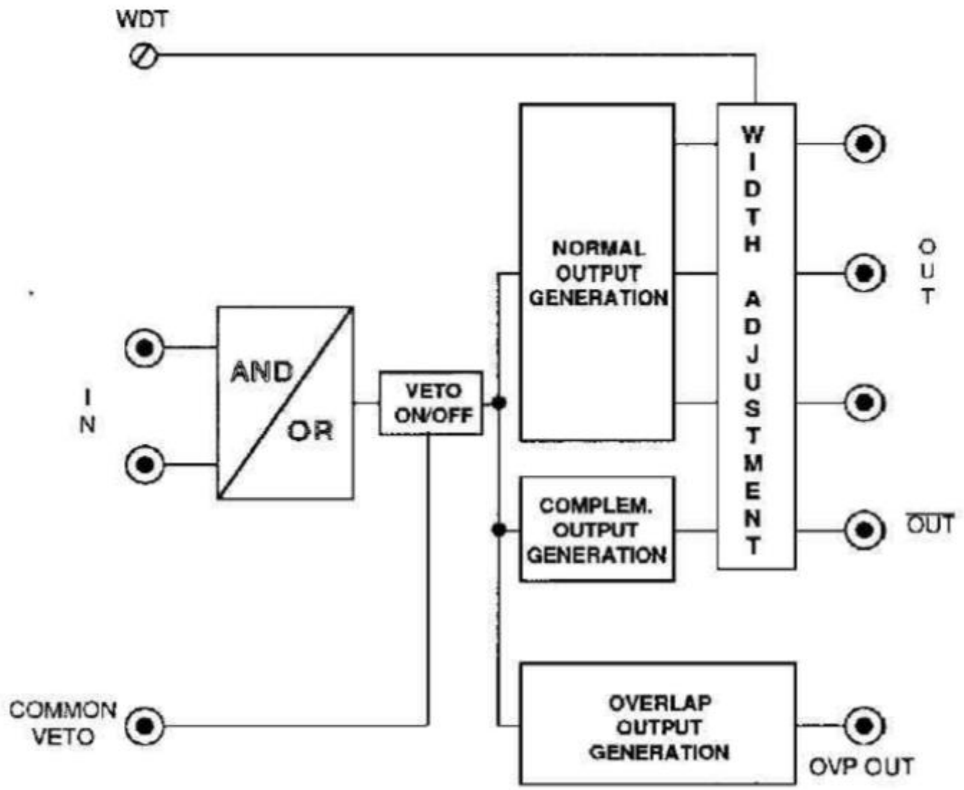


INPUT		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

Logic Unit

https://www.caen.it





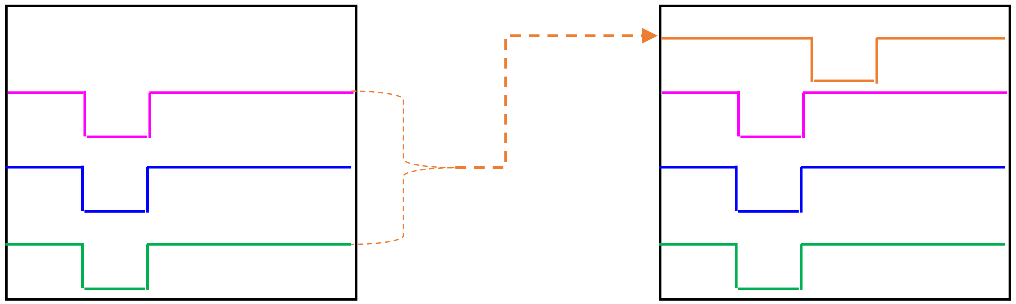
IMPORTANT NOTE:
Unused Outputs require a 50 Ω termination

CAEN N455 Quad Coincidence Logic Unit

Coincidence with 3 inputs

When events occur, **the input signals** from many detectors can be matched with Logic Unit.

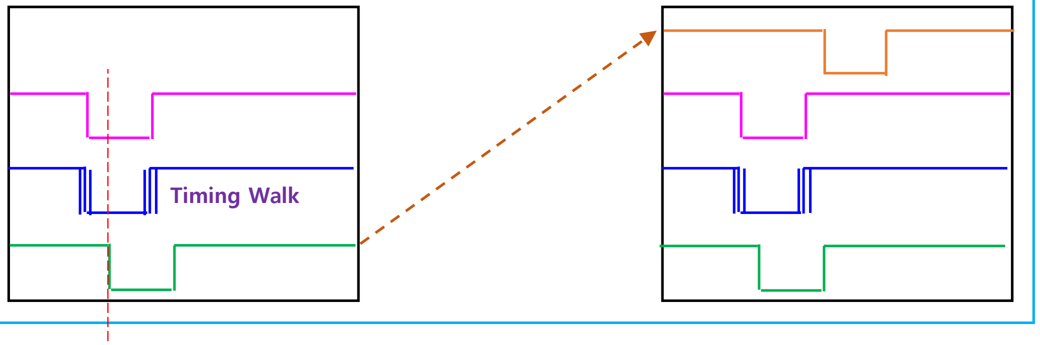
3 coincidence



Coincidence with timing walk

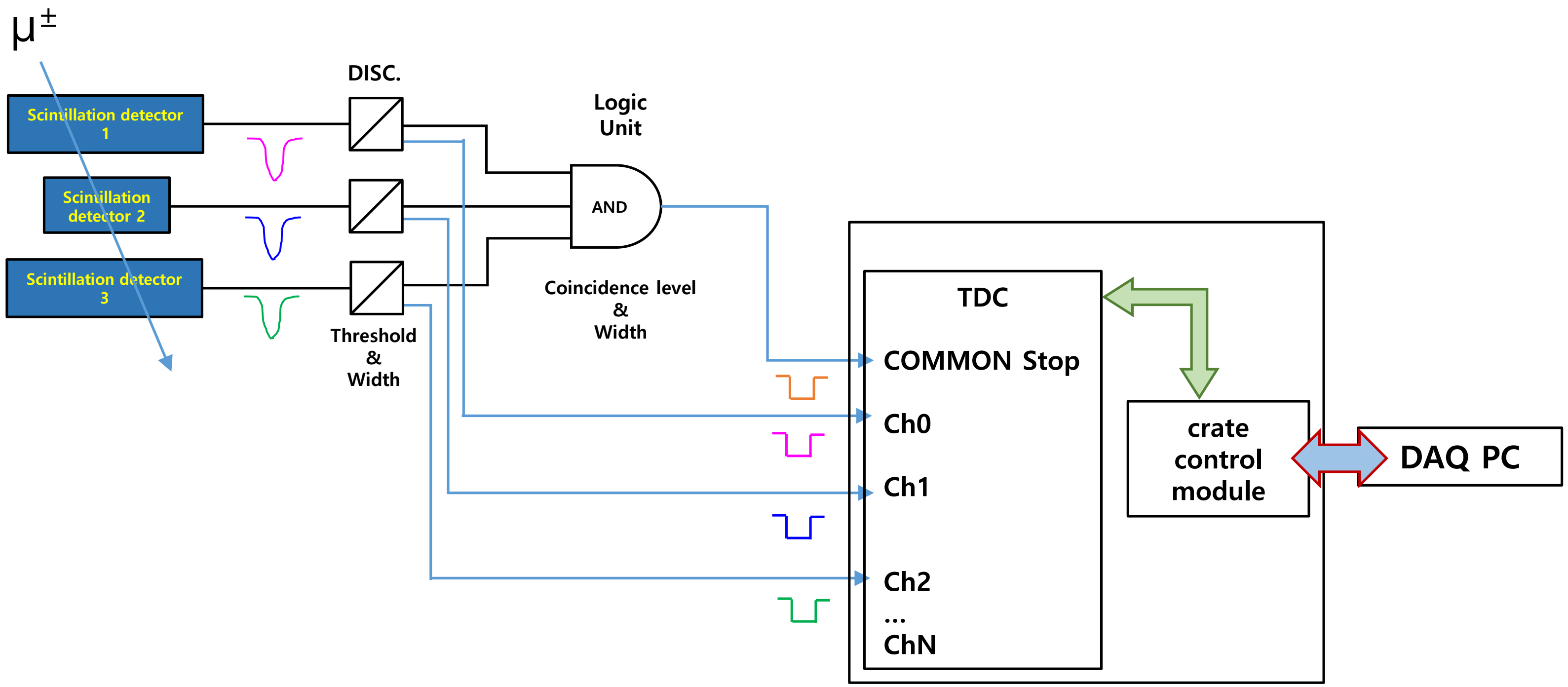
Gate (Ch2) is shaking in time domain, called ***Timing Walk***.

Gate (Ch3) delayed

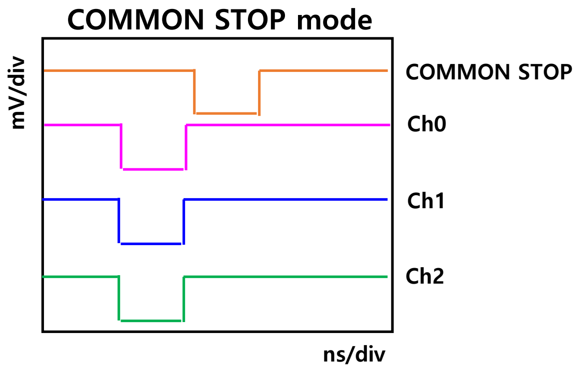


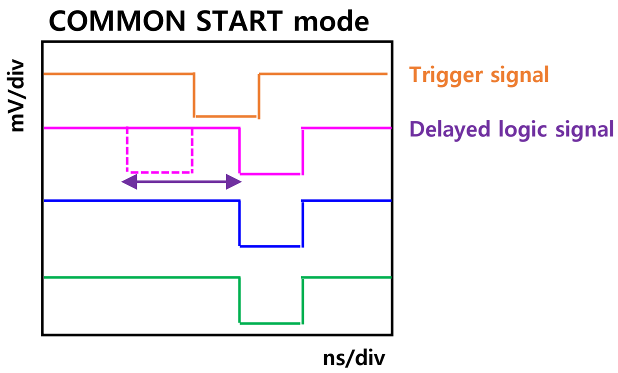
Time measurements with TDC

Scintillation counter/detector:
Scintillator + **P**hoto**M**ultiplier **T**ube (PMT)



Operation mode of TDC: COMMON STOP/START?

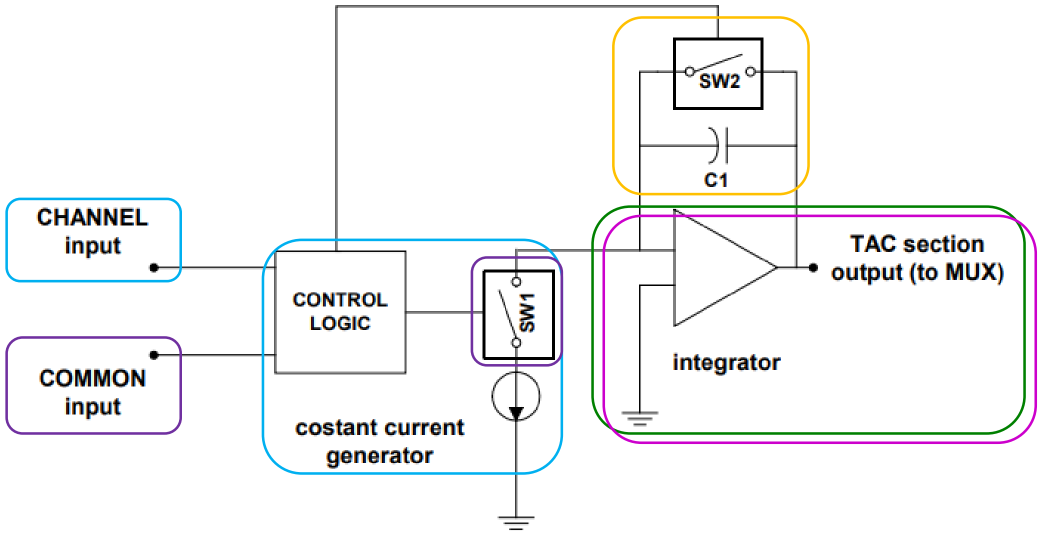




Time-to-Digital Converter (TDC)

How to record time in TDC?

https://www.caen.it



Block diagram of TAC section in CAEN V775N 16ch MultiEvent TDCs

A Start signal closes the **switch SW1** thus allowing a constant current to flow through an integrator; a Stop signal opens the **switch SW1** again.

The constant current generates a **linear ramp voltage which is stopped at an amplitude proportional to the time interval** between Start and Stop pulses. ➔ accumulation on C1

After digitization the **SW2 switch** is closed by the CLEAR signal which allows the discharge of the **capacitor C1**.

Both the COMMON and CLEAR signals are controlled by the CONTROL LOGIC section.

TDC and signal conversion timing

https://www.caen.it

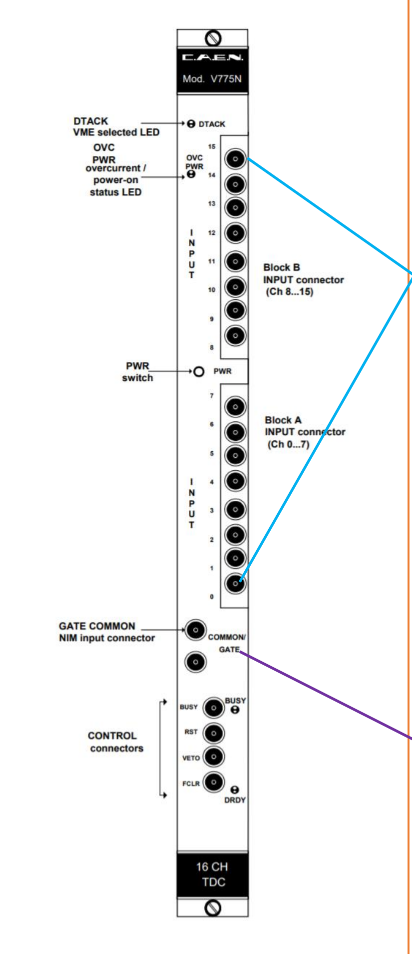
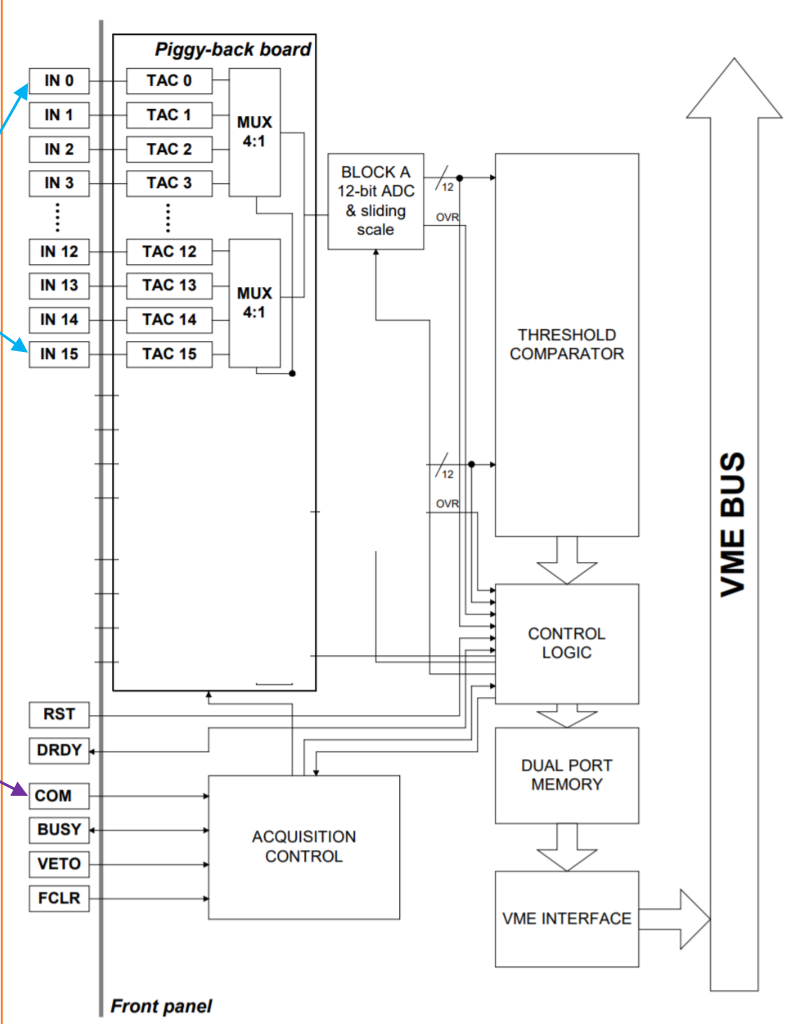


Fig. 3.2: Model V775 N front panel



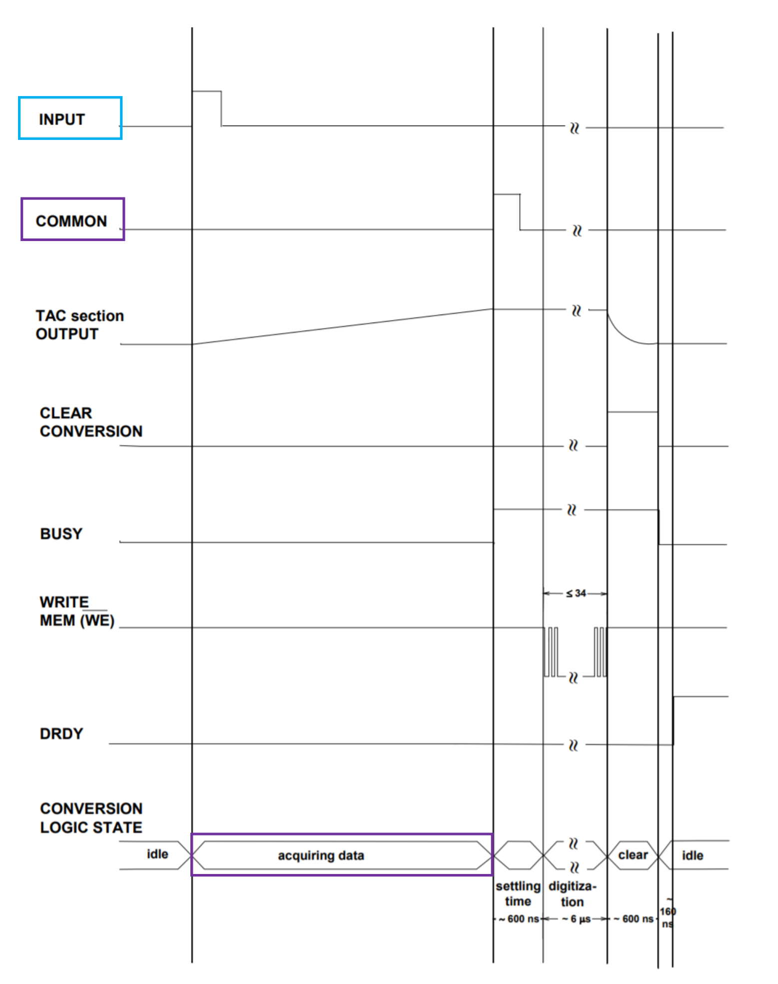


Fig. 2.2: Signal conversion timing in Common Stop mode

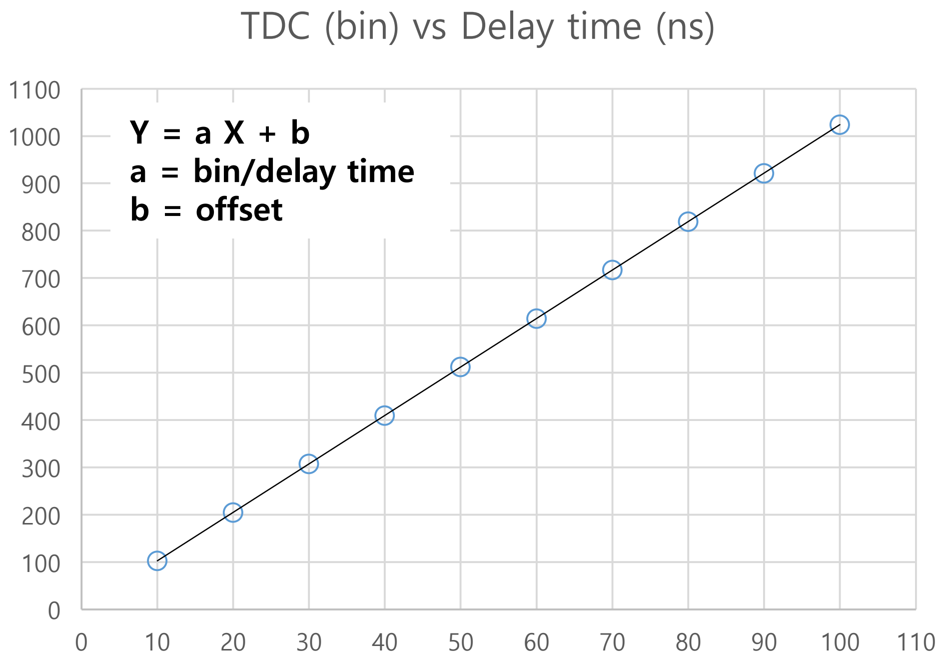
CAEN V775N 16ch MultiEvent TDCs

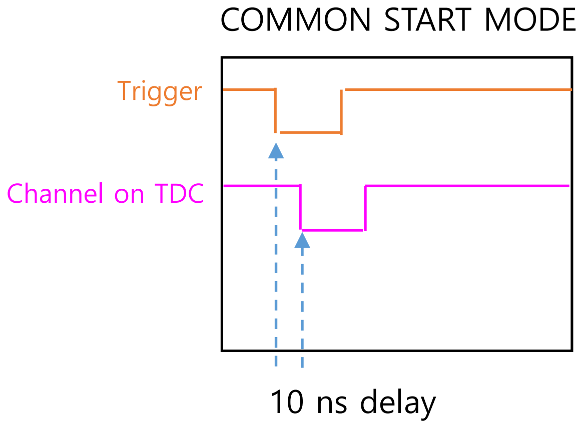
TDC calibration

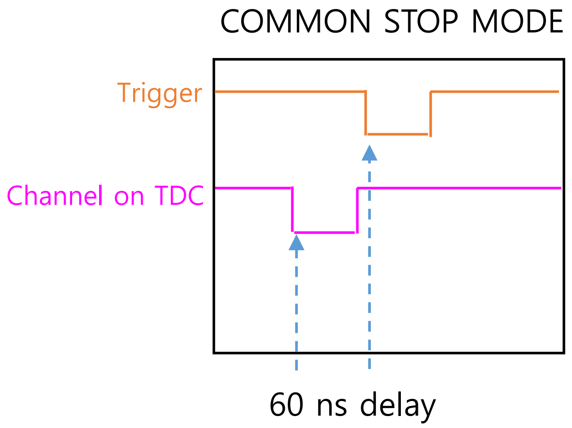
T_full = 100 ns with 10 bit (1024) data set

100	ns
1024	bin
0.09765625	ns/bin

delay (ns)	unit time (ns/bin)	TDC (bin)
10	0.09765625	102.4
20	0.09765625	204.8
30	0.09765625	307.2
40	0.09765625	409.6
50	0.09765625	512
60	0.09765625	614.4
70	0.09765625	716.8
80	0.09765625	819.2
90	0.09765625	921.6
100	0.09765625	1024

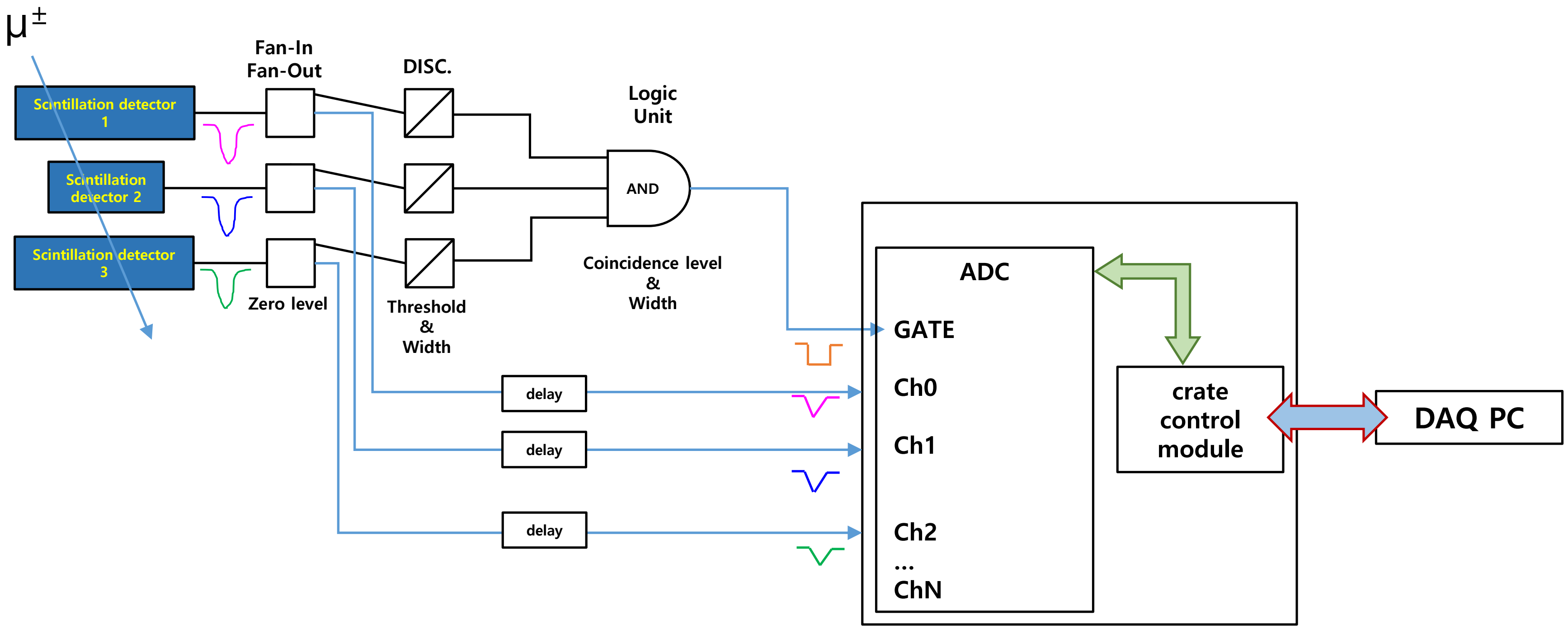




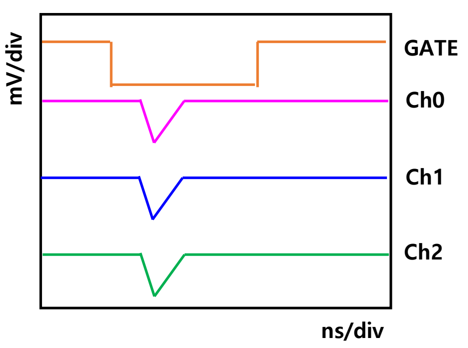


Charge measurements with ADC

Scintillation counter/detector:
Scintillator + **P**hoto**M**ultiplier **T**ube (PMT)

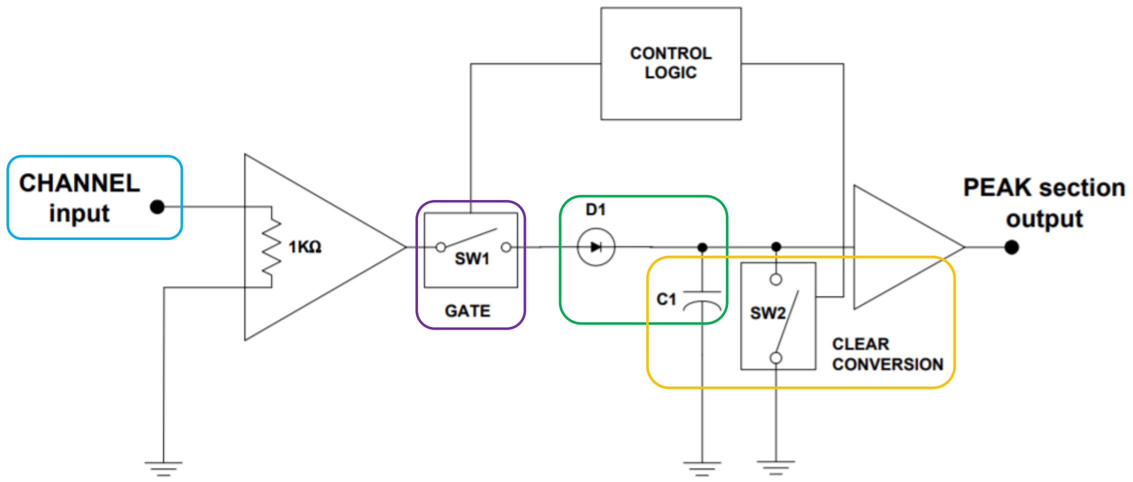


Time domain of signals for ADC



How to record charge in ADC?

https://www.caen.it



Block diagram of PEAK section in CAEN V1785 8ch Dual Range Peak ADC

COMMON STOP mode

The **GATE signal** closes the **switch SW1** thus allowing the **capacitor C1** to be charged as the **diode D1** is forward-biased by the signal.

↓

As the **SW1** is open again, the signal is digitized by the 12-bit ADCs.

↓

After digitization the **SW2 switch** is closed by the CLEAR signal which allows the discharge of the **capacitor C1**.

Both the GATE and CLEAR signals are controlled by the CONTROL LOGIC section.

ADC and signal conversion timing

https://www.caen.it

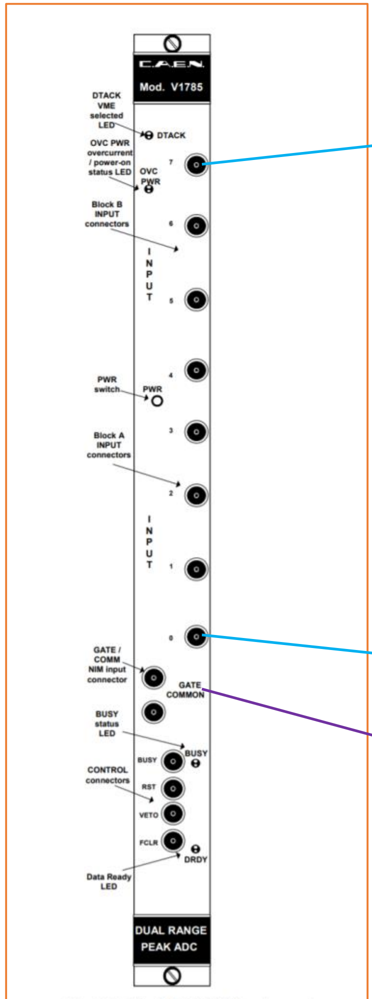


Fig. 3.1: Model V1785 front panel

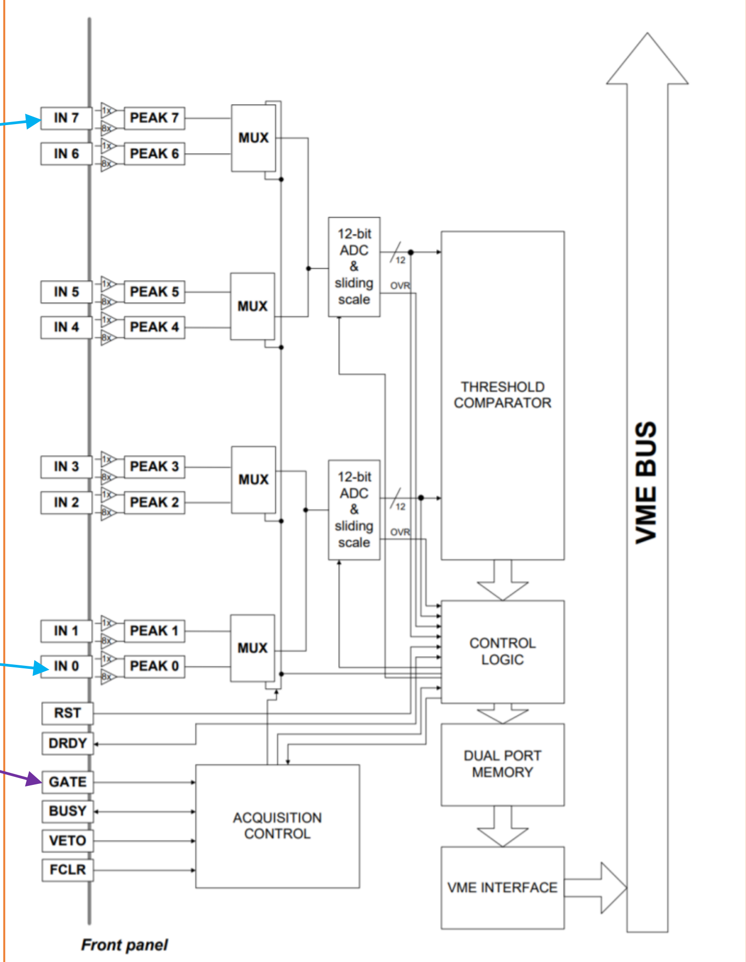


Fig. 1.1: Model V1785 Block Diagram

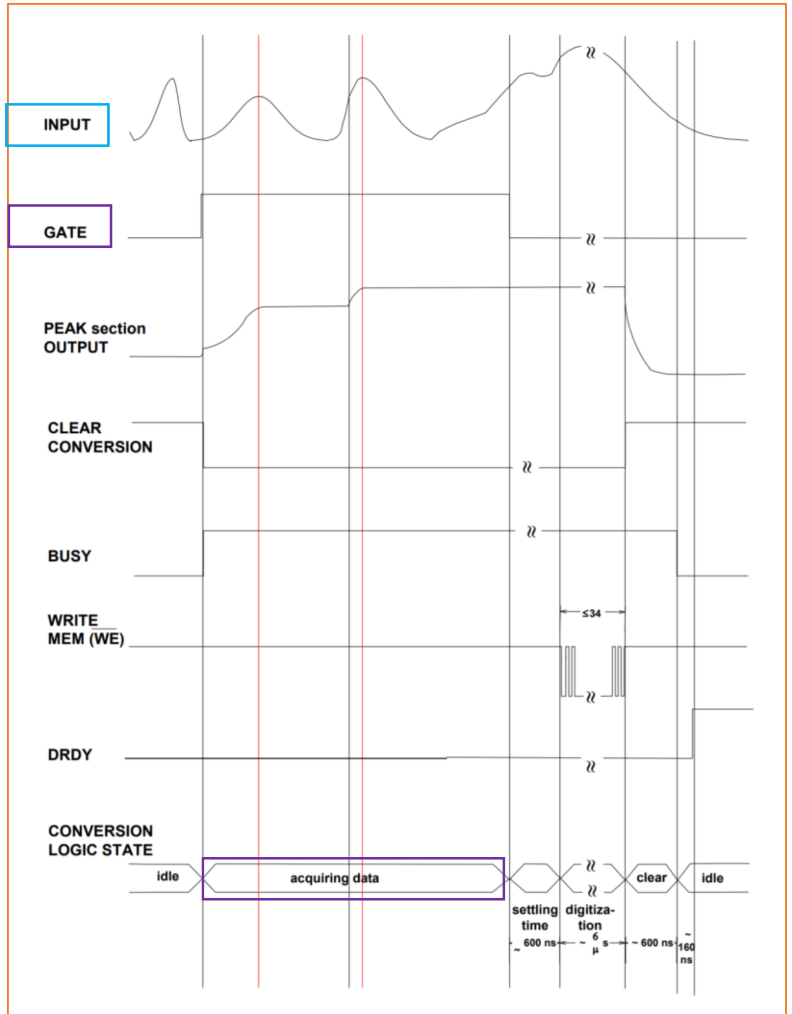


Fig. 2.2: Signal conversion timing

CAEN V1785 8ch Dual Range Peak ADC

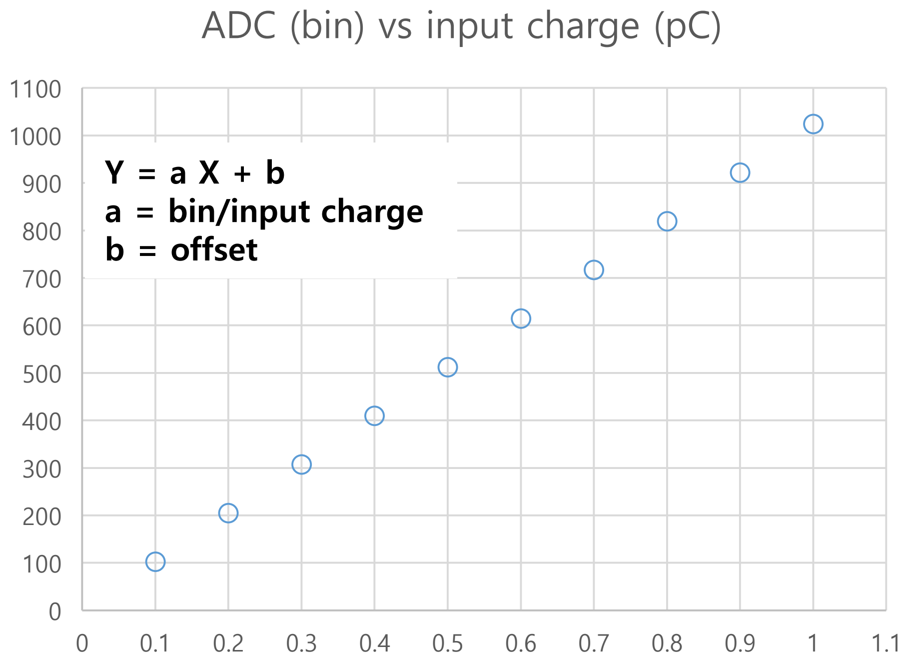
Dual input range: 0 ÷ 4 V / 0 ÷ 500 mV
Gain: 1 mV/count and 125 uV/count for High and Low ranges

ADC calibration

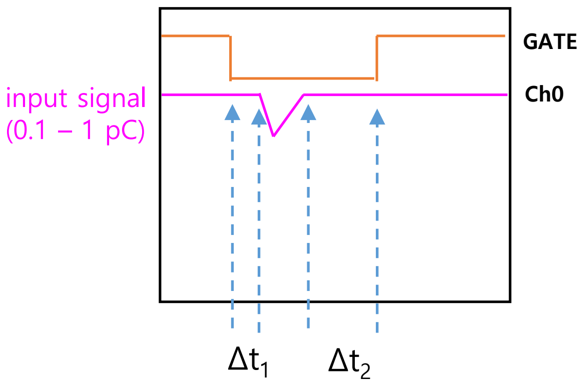
Q_full = 1 pC with 10 bit (1024) data set

1	pC
1024	bin
0.00097656	pC/bin

Q_in (pC)	unit time (pC/bin)	ADC (bin)
0.1	0.000976563	102.4
0.2	0.000976563	204.8
0.3	0.000976563	307.2
0.4	0.000976563	409.6
0.5	0.000976563	512
0.6	0.000976563	614.4
0.7	0.000976563	716.8
0.8	0.000976563	819.2
0.9	0.000976563	921.6
1	0.000976563	1024



Time domain of signals for ADC calibration

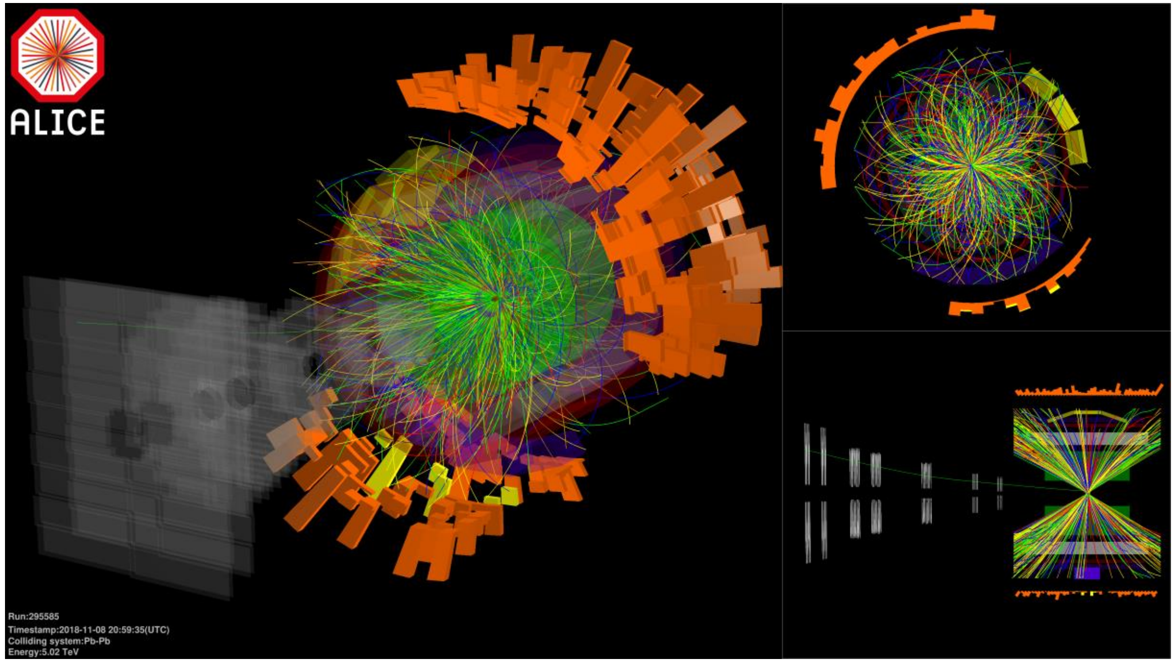


Δt_1 and Δt_2 depends on charge and shape of signal (ex, 10 ns or more).

Summary: Event in HEP experiment

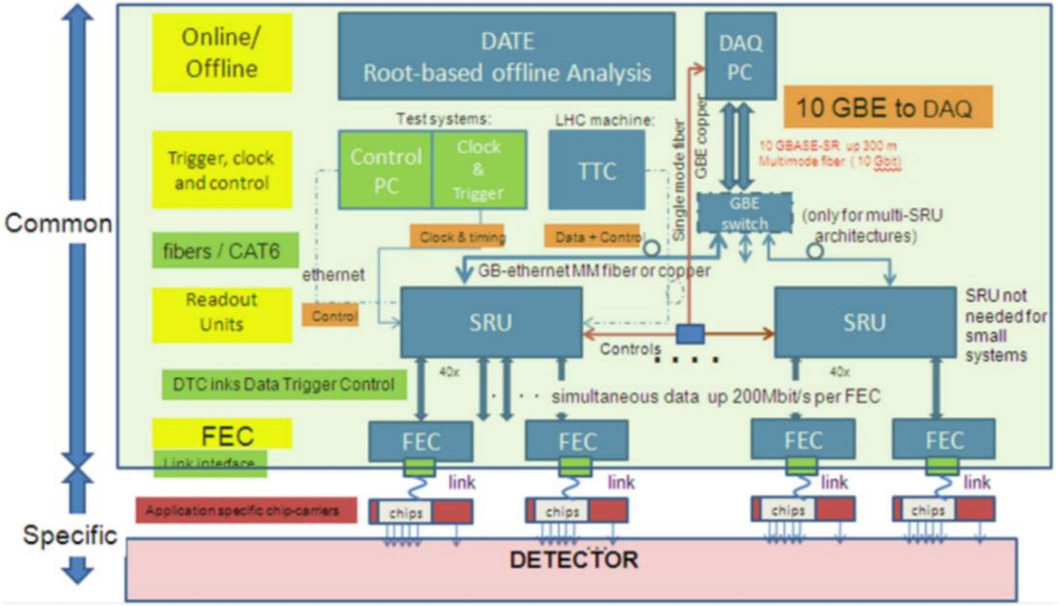
"**Fast Electronics**" are a main component of particle detection system
to see what happens in the HEP experiments.

First Pb collision of ALICE experiment at $\sqrt{s}$ = 5.02 TeV in 2018
https://cds.cern.ch/record/2646381



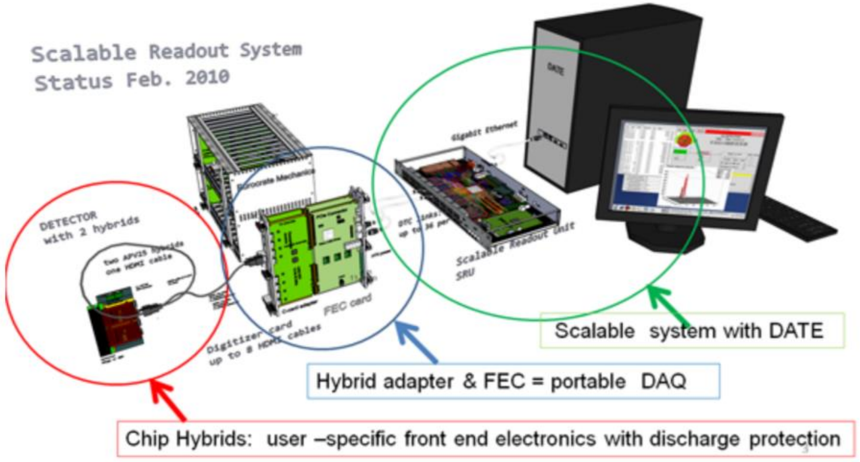
Thank you

RD51 Scalable Readout System (SRS)



https://indico.cern.ch/event/77597/contributions/2088463/attachments/1056845/1506857/RD51-SRS-Description.pdf

physical overview SRS of RD51



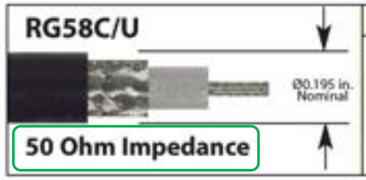
Radio Guide (RG) Cables

http://www.l-com.com/content/Article.aspx?Type=N&ID=10336

Signal transmission

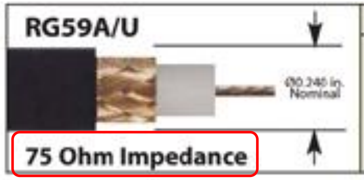
NOMINAL ATTENUATION		
MHz	db/100 ft	db/100m
50	5.8	19.0
100	8.4	27.6
200	12.5	41.0
400	19.0	62.3
1000	34.0	111.5

NOMINAL ATTENUATION		
MHz	db/100 ft	db/100m
50	5.6	18.4
100	8.3	27.2
200	12.0	39.4
400	17.5	57.4
1000	29.0	95.1

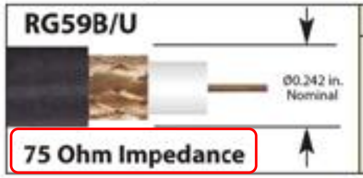


NOMINAL ATTENUATION		
MHz	db/100 ft	db/100m
50	3.3	10.8
100	4.9	16.1
200	7.3	23.9
400	11.0	36.1
1000	20.0	65.6

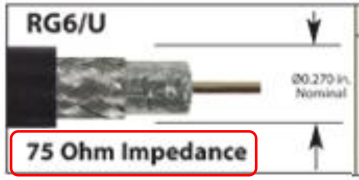
HV transmission



NOMINAL ATTENUATION		
MHz	db/100 ft	db/100m
50	2.8	9.2
100	4.0	13.1
200	5.9	19.4
400	8.5	27.9
1000	13.8	45.3



NOMINAL ATTENUATION		
MHz	db/100 ft	db/100m
50	2.4	7.9
100	3.4	11.1
200	4.9	16.1
400	7.0	23.0
1000	12.0	39.3



NOMINAL ATTENUATION		
MHz	db/100 ft	db/100m
50	1.5	4.9
100	2.1	6.9
200	3.1	10.2
400	4.5	14.8
1000	7.3	23.9

How fast signals move in cables? v_{signal} = ~5 ns/m

	c (m/s)	Velocity Fraction (%)	v (m/s)	v (m/ns)	v (cm/ns)	Connector type
Vacuum	3.00E+08	1	3.00E+08	0.300	30.0	
RG174	3.00E+08	0.66	1.98E+08	0.198	19.8	**LEMO**
RG316	3.00E+08	0.79	2.37E+08	0.237	23.7	**LEMO**
RG58	3.00E+08	0.66	1.98E+08	0.198	19.8	**BNC**

Power loss $\alpha_P(dB/km) = \frac{10}{L} log_{10}^{(P_1/P_2)}$

α_P = power attenuation, or loss between source and destination, unit (dB/km)
P_1 = power at the beginning (Source), unit (W)
P_2 = power at the end (Destination), unit (W)
L = distance between P_1 and P_2, unit (km)

If P_1 = 1 W, P_2 = 0.5 W, and L = 0.1 km, $\alpha_P = \frac{10}{0.1} log_{10}^{(1/0.5)}$ = 3.01 dB/100m

Power at the distance (L) : $P_2 = P_1 \cdot \exp(-\alpha_P L)$

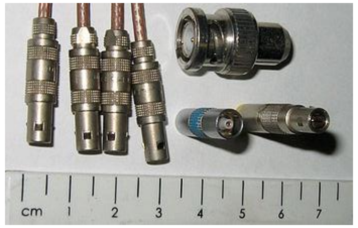
RG58/U: 20 AWG (Φ0.812 mm) bare copper (28.5 pF/ft)
RG58A/U: 20 AWG standard thin copper (30.8 pF/ft)
RG58C/U: same as RG58A/U but not same outer jacket material

RG59A/U: 22 AWG (Φ0.644 mm) bare compacted copper
RG59B/U: 22 AWG solid bare copper covered steel

U: Universal
AWG: American Wire Gauge

Connectors for signal and high voltage

Signal connection
LEMO **(**company founder, engineer **Lé**on **Mo**uttet**)**
name of an electronic and fibre optic connector manufacturer
push-pull connectors
NIM, CAMAC, VME, detector, and etc




BNC **(Bayonet Neill-concelman) connector:** miniature quick connect/disconnect
50 or 75 ohm impedance
frequencies below 4 GHz
voltage below 500 V
NIM, audio, video, detector and etc

SMA (Sub Miniature version A): semi-precision coaxial RF connectors
screw-type coupling mechanism
male Φ0.312 in (Φ7.9 mm)
0-18 GHz passband (some up to 26.5 GHz)
detector and etc


High voltage connection
MHV (miniature high voltage): type of RF connector used for terminating a coaxial cable

SHV (**safe high voltage**) **connector:** safer handling HV than other connectors
standard: up to5 kV (5 A)
higher-version: 20 kV or more
NIM, detector, and etc

CAMAC

Computer Aided Measurement And Control (CAMAC)**:** a joint specification of the U.S. NIM and the European ESONE committees for a modular, high-performance, real-time data acquisition and control system concept.

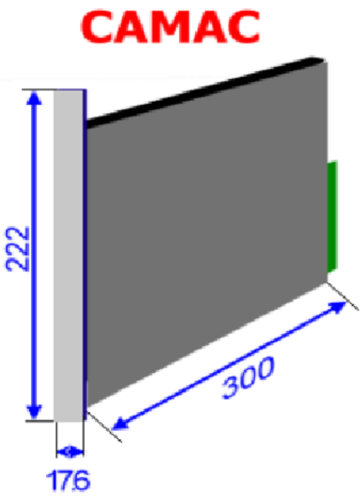
CAMAC was introduced in 1969 by ESONE and fully defined in 1971 with the standards EUR4100 and EUR4600 / IEEE Standard 583-1982 (reaffirmed 1994) “Modular Instrumentation and Digital Interface System (CAMAC)”.

It represents a complementation of the NIM standard for computer based experiment control and data acquisition. Main field of CAMAC use are computer based control and data acquisition systems in nuclear and high-energy physics experiments but in the past also in industrial applications, aerospace, and defense test systems.

All CAMAC bus signals are TTL logic levels as given in the following table:

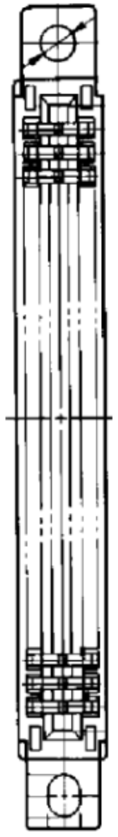
	Logic 0	Logic 1
Input must accept	+2.0 to 5.5V	0 to +0.8V
Output must accept	+3.5 to 5.5V	0 to +0.5V

Size: H222xW17.6xD300 mm (except backplane power connector)



CAMAC Pin assignment (viewed from front)

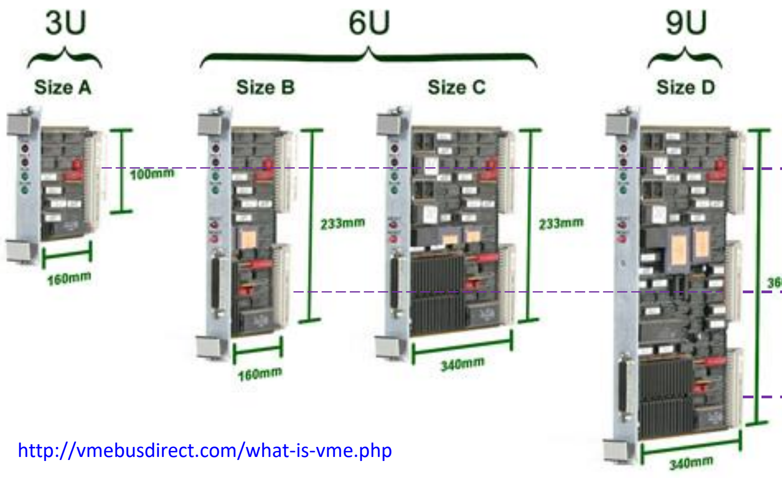
Controller station		Normal station	
P1	B	P1	B
P2	F16	P2	F16
P3	F8	P3	F8
P4	F4	P4	F4
P5	F2	P5	F2
X	F1	X	F1
I	A8	I	A8
C	A4	C	A4
P6	A2	N	A2
P7	A1	L	A1
S1	Z	S1	Z
S2	Q	S2	Q
L24	N24	W24	W23
L23	N23	W22	W21
L22	N22	W20	W19
L21	N21	W18	W17
L20	N20	W16	W15
L19	N19	W14	W13
L18	N18	W12	W11
L17	N17	W10	W9
L16	N16	W8	W7
L15	N15	W6	W5
L14	N14	W4	W3
L13	N13	W2	W1
L12	N12	R24	R23
L11	N11	R22	R21
L10	N10	R20	R19
L9	N9	R18	R17
L8	N8	R16	R15
L7	N7	R14	R13
L6	N6	R12	R11
L5	N5	R10	R9
L4	N4	R8	R7
L3	N3	R6	R5
L2	N2	R4	R3
L1	N1	R2	R1
-12	-24	-12	-24
NC	-6	NC	-6
NC	NC	NC	NC
Y1	E	Y1	E
12	24	+12	+24
Y2	6	Y2	6
0	0	0	0



VME

VersaModular Eurocard (VME):

Height ➔



http://vmebusdirect.com/what-is-vme.php

Width of VME modules: 20.3 mm

1 U rack size = 4.445 cm

VME bus J1/P1 Pinouts

PIN	ROW A	ROW B	ROW C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

VME bus J2/P2 Pinouts

PIN	ROW A	ROW B	ROW C
1	User Defined	+5	User Defined
2	User Defined	GND	User Defined
3	User Defined	RESERVED	User Defined
4	User Defined	A24	User Defined
5	User Defined	A25	User Defined
6	User Defined	A26	User Defined
7	User Defined	A27	User Defined
8	User Defined	A28	User Defined
9	User Defined	A29	User Defined
10	User Defined	A30	User Defined
11	User Defined	A31	User Defined
12	User Defined	GND	User Defined
13	User Defined	+5	User Defined
14	User Defined	D16	User Defined
15	User Defined	D17	User Defined
16	User Defined	D18	User Defined
17	User Defined	D19	User Defined
18	User Defined	D20	User Defined
19	User Defined	D21	User Defined
20	User Defined	D22	User Defined
21	User Defined	D23	User Defined
22	User Defined	GND	User Defined
23	User Defined	D24	User Defined
24	User Defined	D25	User Defined
25	User Defined	D26	User Defined
26	User Defined	D27	User Defined
27	User Defined	D28	User Defined
28	User Defined	D29	User Defined
29	User Defined	D30	User Defined
30	User Defined	D31	User Defined
31	User Defined	GND	User Defined
32	User Defined	+5V	User Defined

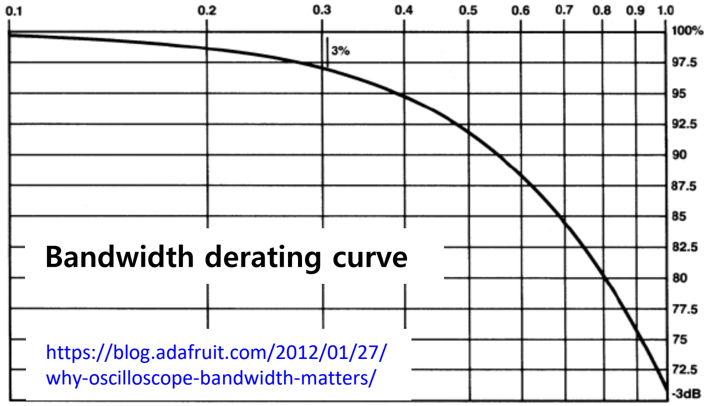
VME bus J3/P3 Pinouts

PIN	ROW A	ROW B	ROW C
1	+5V	User Defined	GND
2	+5V	User Defined	GND
3	+5V	User Defined	GND
4	+5V	User Defined	GND
5	+5V	User Defined	GND
6	+5V	User Defined	GND
7	+5V	User Defined	GND
8	+5V	User Defined	GND
9	+5V	User Defined	GND
10	+5V	User Defined	GND
11	+5V	User Defined	GND
12	+5V	User Defined	GND
13	+5V	User Defined	GND
14	+5V	User Defined	GND
15	+5V	User Defined	GND
16	+5V	User Defined	GND
17	+5V	User Defined	GND
18	+5V	User Defined	GND
19	+5V	User Defined	GND
20	+5V	User Defined	GND
21	+5V	User Defined	GND
22	+5V	User Defined	GND
23	+5V	User Defined	GND
24	+5V	User Defined	GND
25	+5V	User Defined	GND
26	+12V	User Defined	+12V
27	+12V	User Defined	+12V
28	-12V	User Defined	-12V
29	-12V	User Defined	-12V
30	-5V	User Defined	-5V
31	-5V	User Defined	-5V
32	-5V	User Defined	-5V

Oscilloscope

Bandwidth:

maximum frequency of an input signal which can pass through the analog front end of the scope with minimal amplitude loss



If you require 3% accuracy, you need to derate it by a factor of ~0.3x, so a **350 MHz scope** can **accurately measure 105 MHz to 3%**.

Sampling rate:

maximum number of samples per second