Design of PiN sensor based on TCAD simulation and ITS3 plan of Inha University

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Silicon sensor seminar

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FAZIA(Forward-angle A and Z Identification Array) experiment

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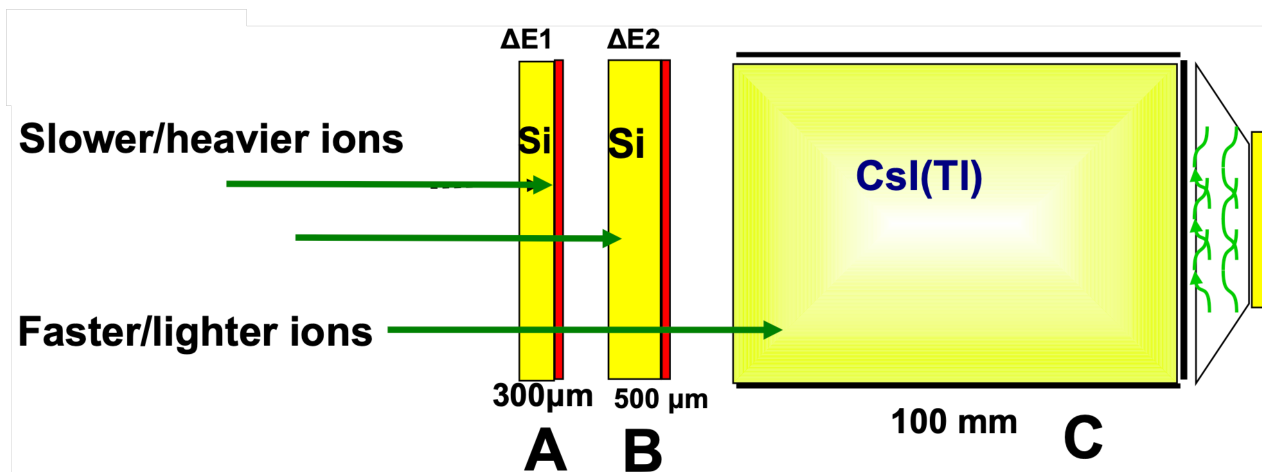
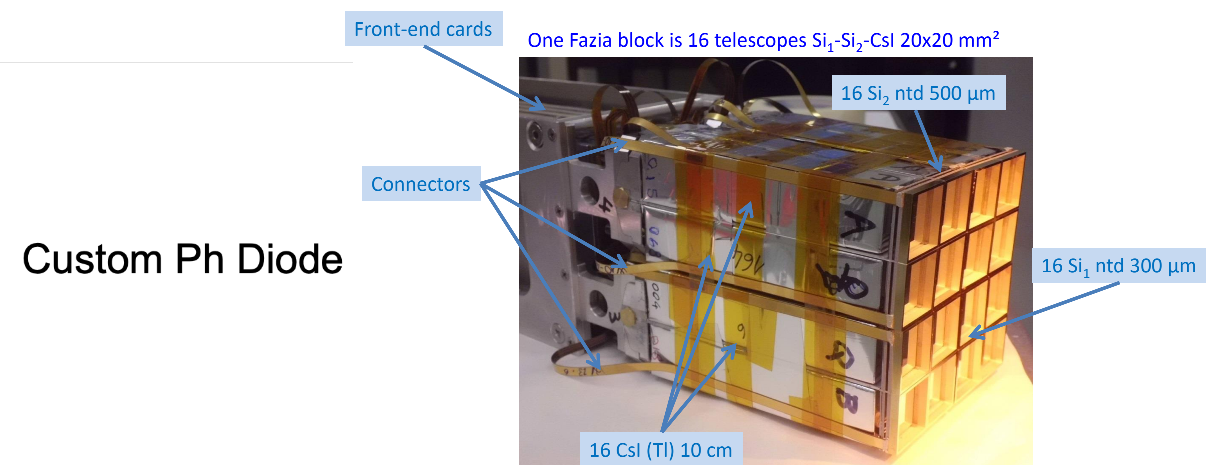
- FAZIA experiment helps understanding Equation of State and constraining the Nuclear symmetry energy
- FAZIA detector is a telescope consisting of two silicon sensors and one scintillator
- Particle identification and isotope separation via ΔE–E correlation
- To upgrade two silicon sensors, we calculated the physical properties of the sensor based on TCAD simulation.





Cross section area of telescope 2cm x 2cm

Synopsys TCAD(Technology Computer Aided Design) tool

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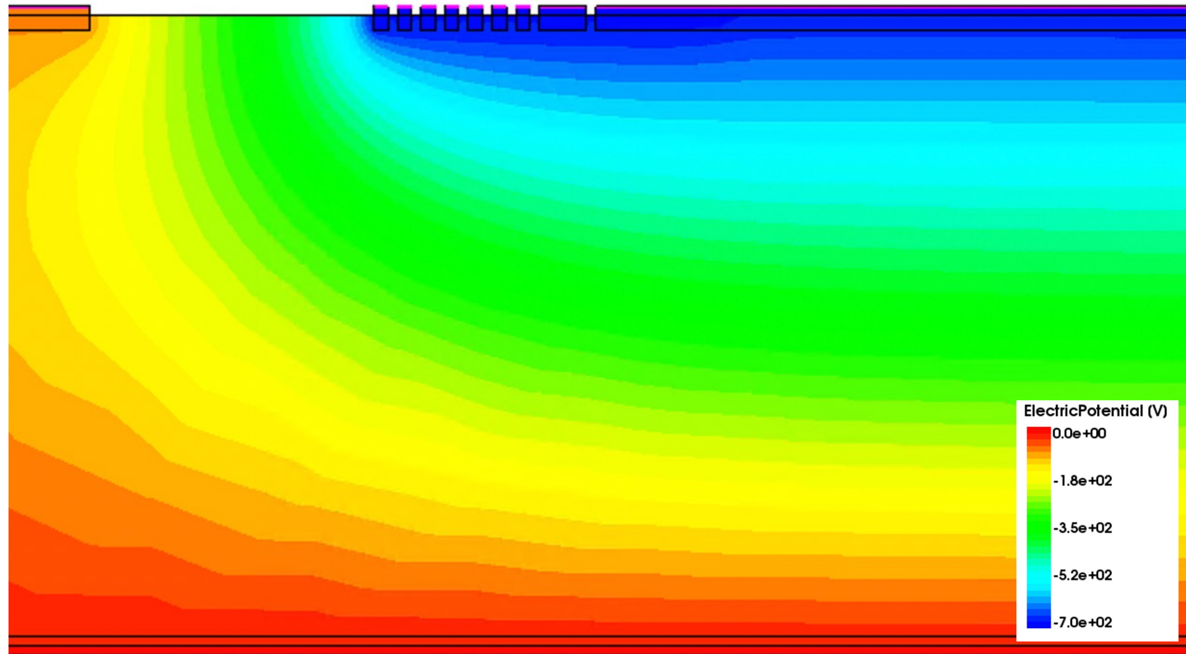

- Electrostatic Potential

$$\nabla \cdot (\varepsilon \nabla \phi + \vec{P}) = -q(p - n + N_{\mathrm{D}} - N_{\mathrm{A}}) - \rho_{\mathrm{trap}}$$

- Carrier transport model

$$\nabla \cdot \overrightarrow{J_{\mathrm{n(p)}}} = q(R_{\mathrm{net,n(p)}} - G_{\mathrm{net,n(p)}}) + q\frac{\partial n(p)}{\partial t}$$

- Drift-diffusion model

$$\overrightarrow{J_{\mathrm{n(p)}}} = -n(p)\mu_{\mathrm{n(p)}} \nabla \Phi_{\mathrm{n(p)}}$$ by Einstein relation

ε : electrical permittivity

$\vec{P}$: ferroelectric polarization

n(p) : electron(hole) density

q : elementary charge

$\mu_{\mathrm{n(p)}}$: electron(hole) carrier mobility

$R_{\mathrm{net,n(p)}}$: electron(hole) net recombination rate

$G_{\mathrm{net,n(p)}}$: electron(hole) net generation rate

$\overrightarrow{J_{\mathrm{n(p)}}}$: electron(hole) current density

$\Phi_{\mathrm{n(p)}}$: electron(hole) quasi_Fermi potential

N_{D} (N_A) : concentration of ionized donors(acceptors)

Simulation setup

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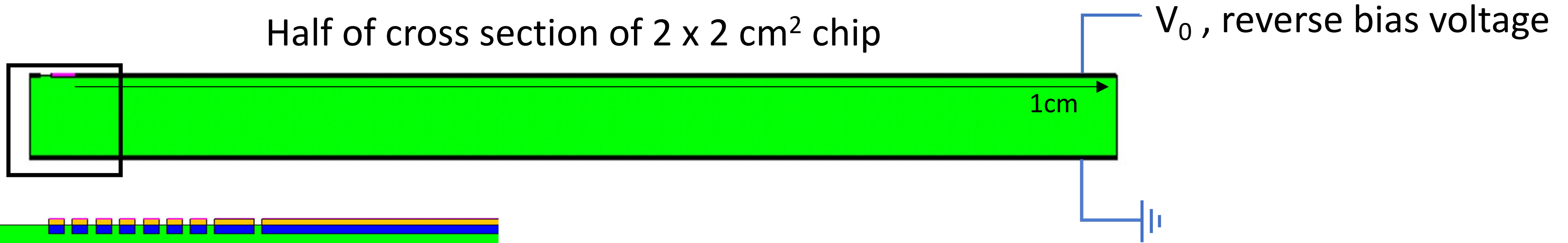
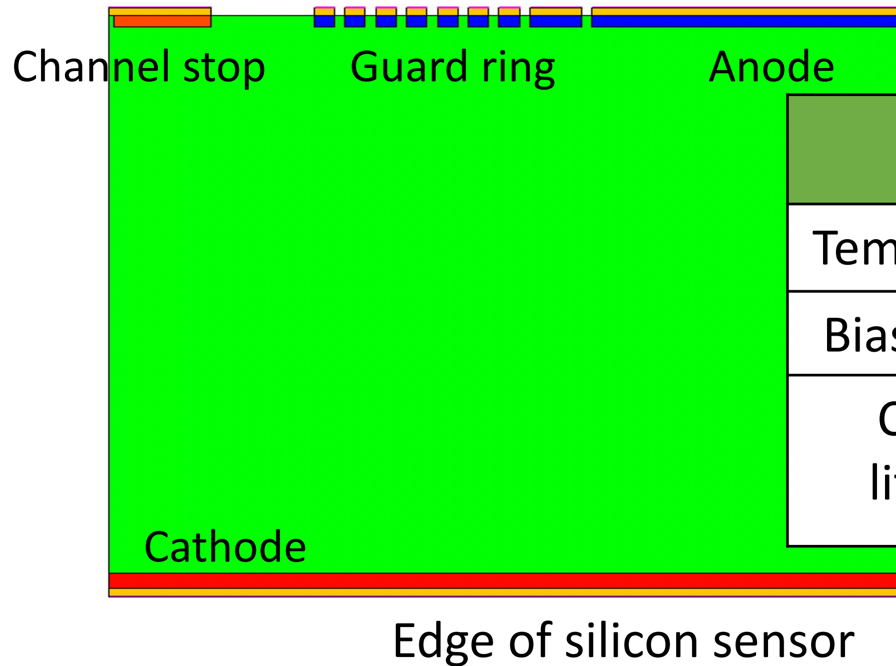


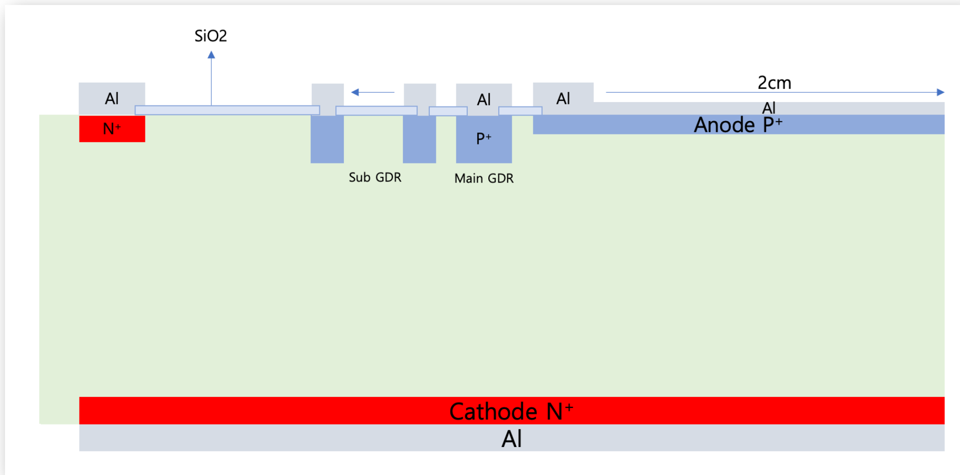


Edge of silicon sensor

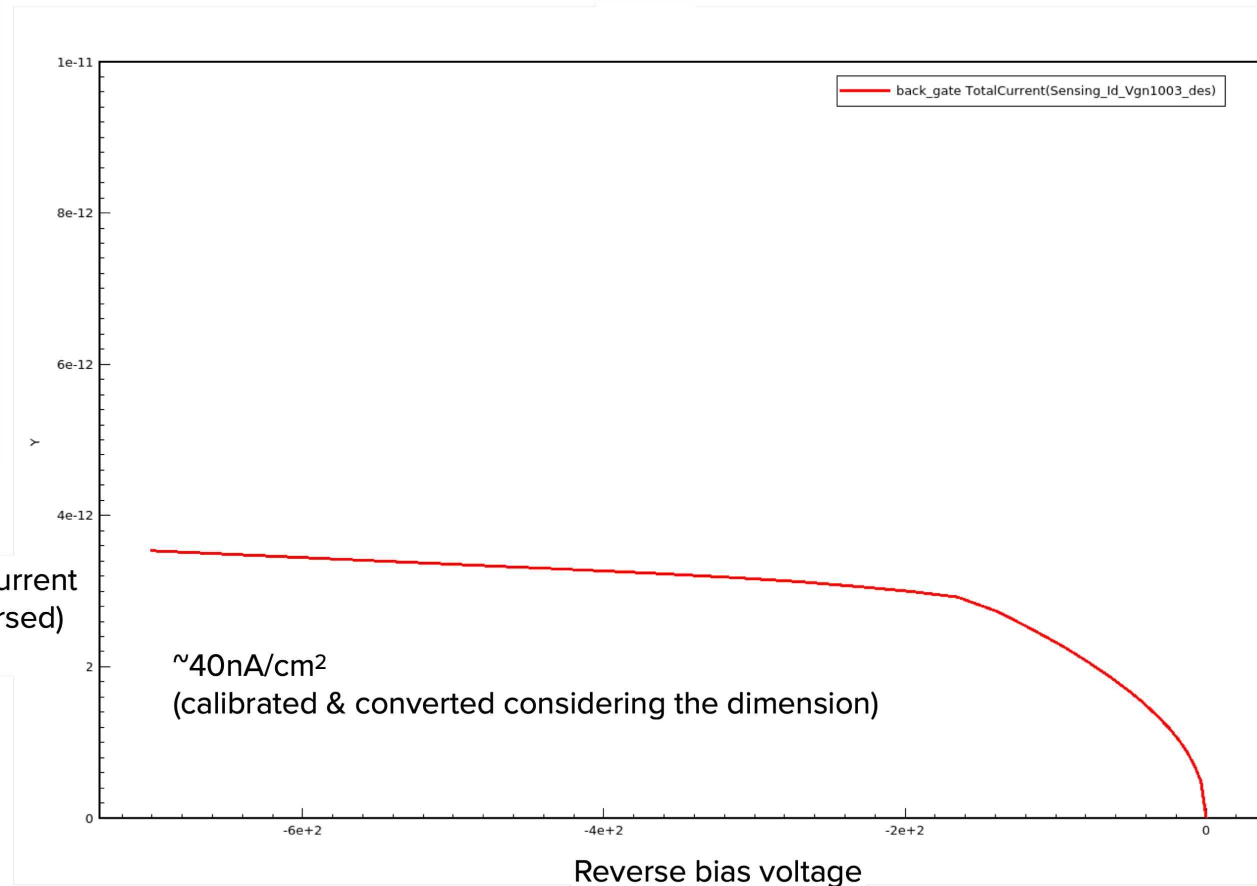
Input parameter				
Temperature	300K		Doping density	
Bias voltage	0 ~ -700V		(blue)	P^+ Boron
Carrier lifetime	electron	$1x10^{-4}s^{-1}$	(green)	N^- Phosphorus
	hole	$3x10^{-4}s^{-1}$	(red)	N^+ Phosphorus

Design of PiN sensor using TCAD simulation

Leakage current result with the final design



➢ We calculated the leakage current of the final design based on the calibrated parameters.



Sensor fabrication

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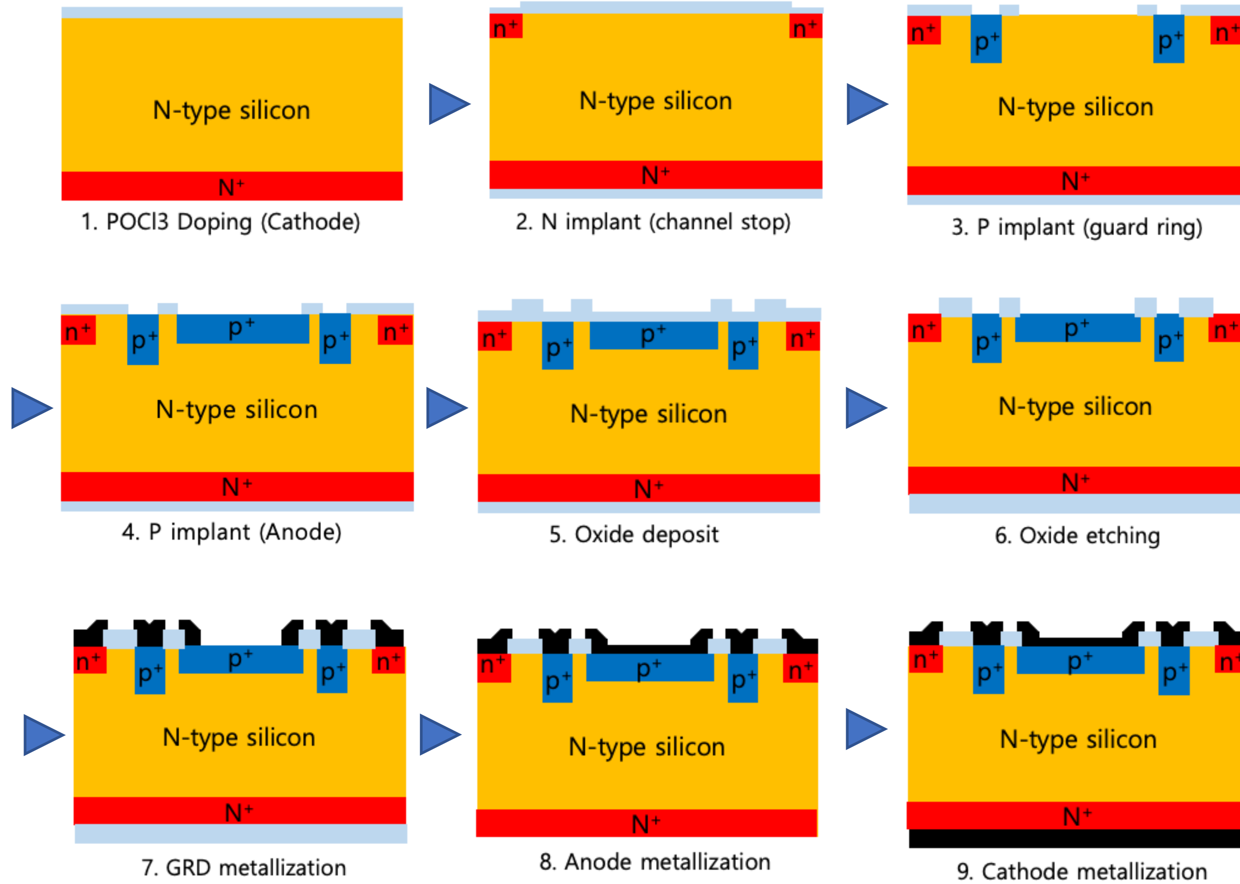
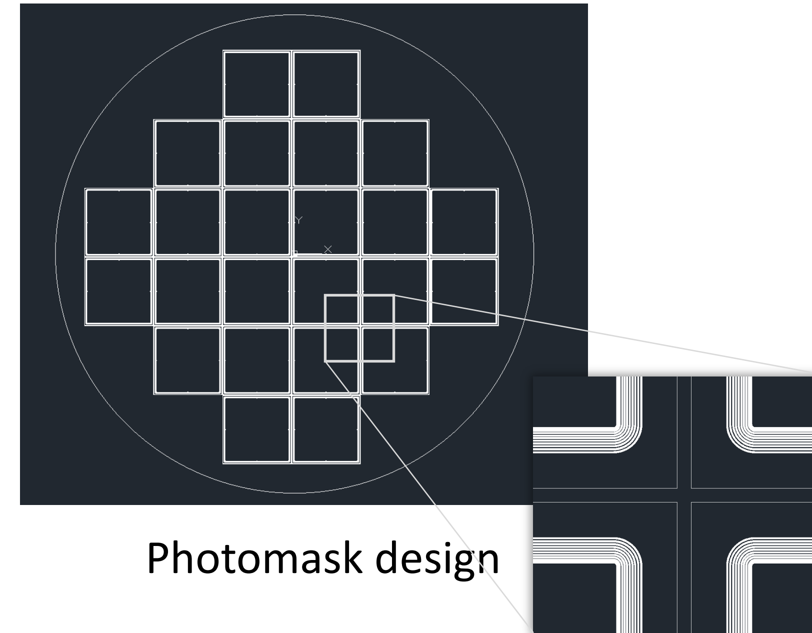


fabrication flow

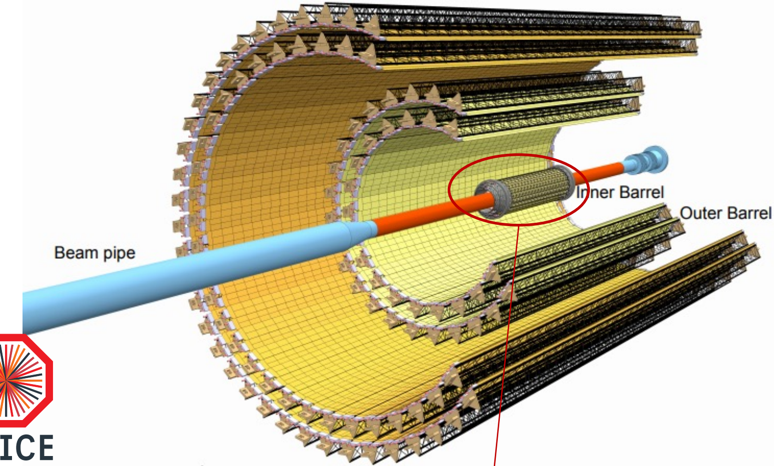


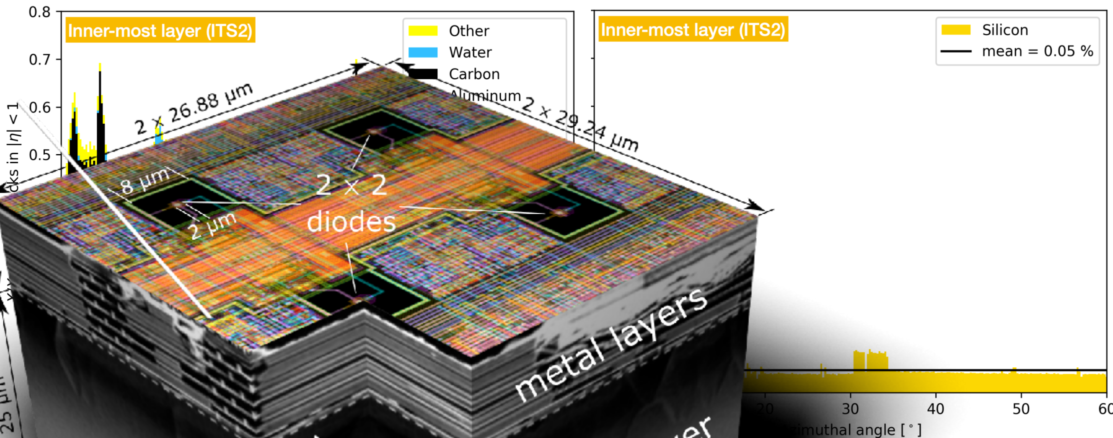
Photomask design

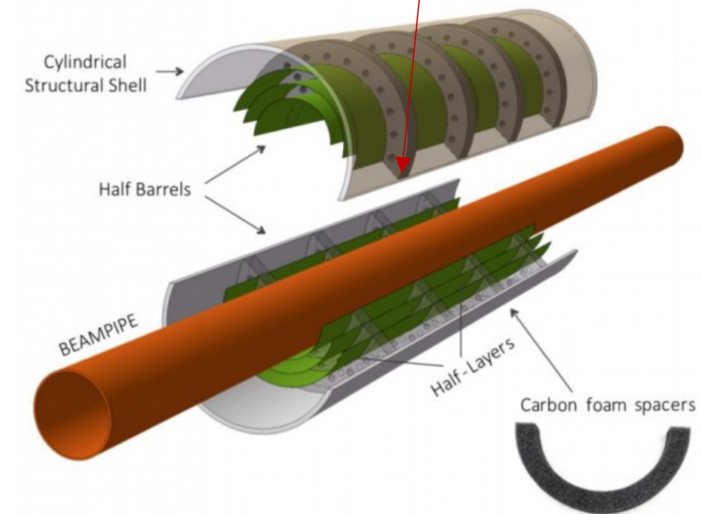
- design process flow & photomask for fabrication

ALICE ITS3 upgrade

- Large size chip based on stitching technology
- Thickness ~ 50um → Si wafer can be bent
- Lower material budget → Leave only silicon
- Expect the improvement of tracking precision and efficiency at low p_T







ALICE3 upgrade

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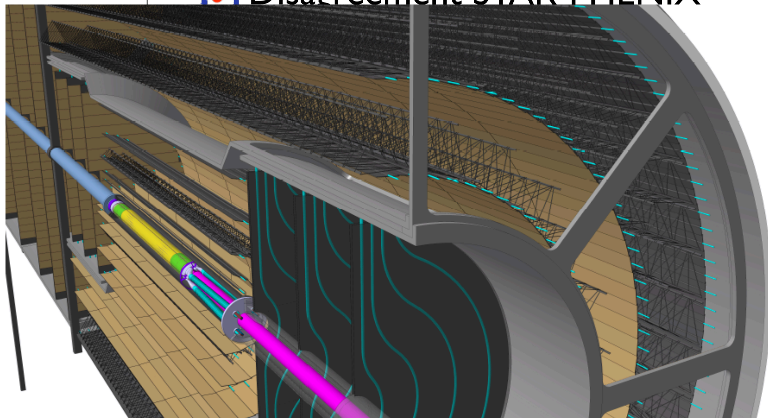
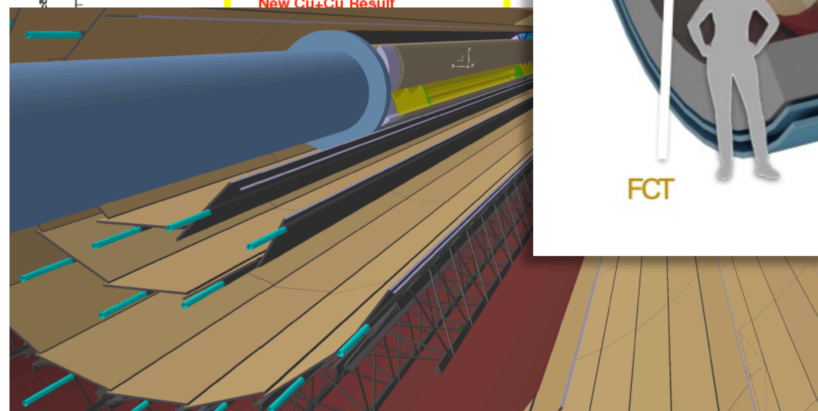
- All detectors consist of silicon sensors
- Outer tracker is CMOS trajectory tracking detector
  - Large coverage (-4 < η < +4)
  - Low power consumption : ~20mW/cm2

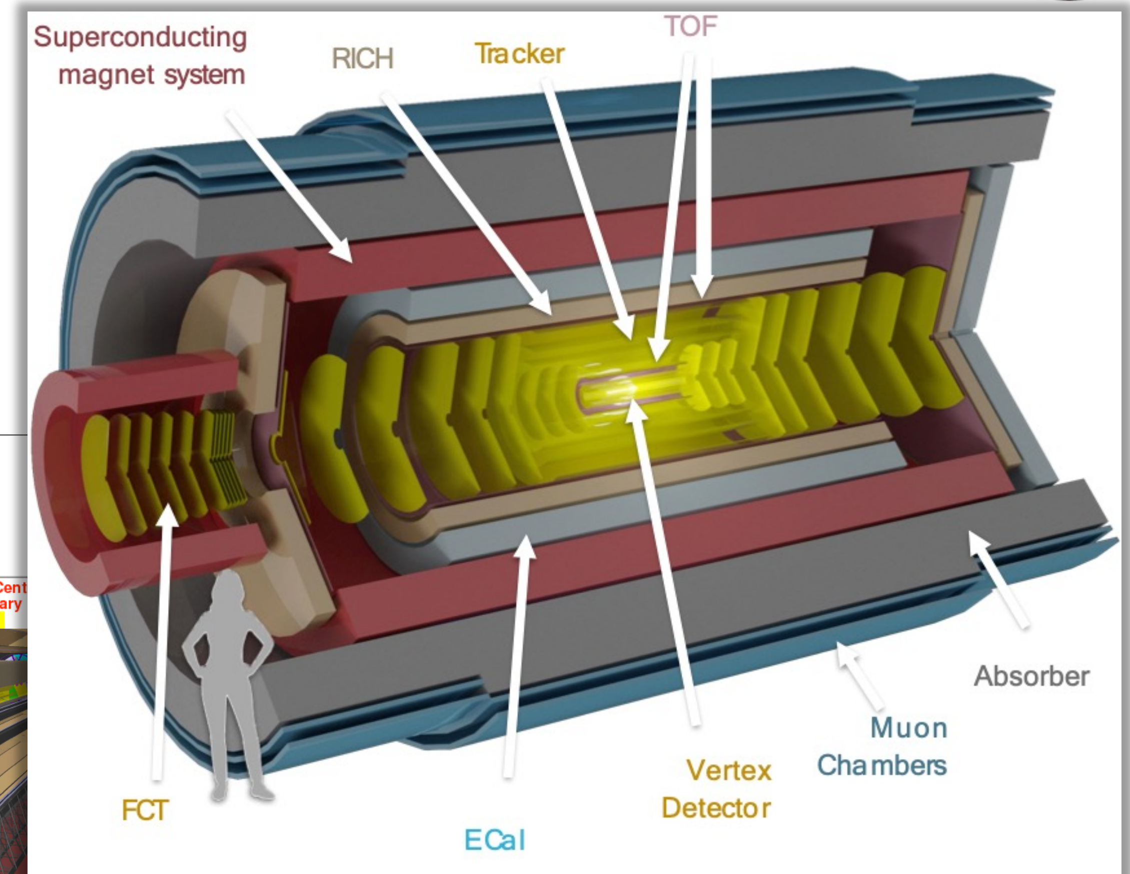
What about RHIC results

☑ Disagreement STAR-PHENIX

STAR Au+Au Cent
STAR Preliminary
New Cu+Cu Result







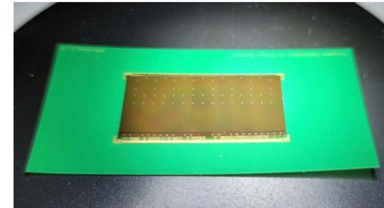
level of light quark. *Predictions contradicted!.*

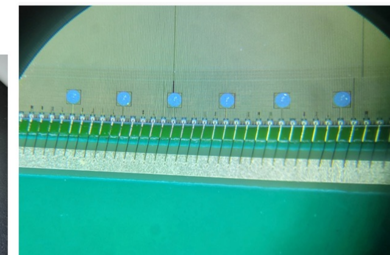
$\hat{q} = 10GeV^2/fm$
$\hat{q} = 14GeV^2/fm$
STAR

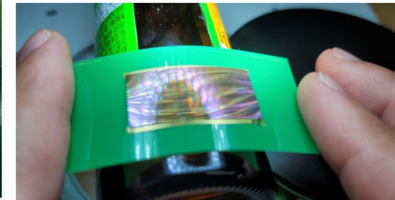
Bent ITS3 chip test at Inha Univ, PNU, (SKKU is joining)

- Involved people at this moment
- 4 graduate/undergraduate students (Giyeong Kim*, Hangil Jang, Sungwoon Choi, Yongjun Choi), 1 post-doc (Jiyoung Kim, contact person), 3 Professors (In-Kwon Yoo, MinJung Kweon, Sanghoon Lim)

- Plan for ITS3 project of Inha Univ.
- Characterization measurement with bent chip using Flexible Printed Circuit (made in MEMSPACK)
- The company suggested a way to do bonding first and then bending the chip later



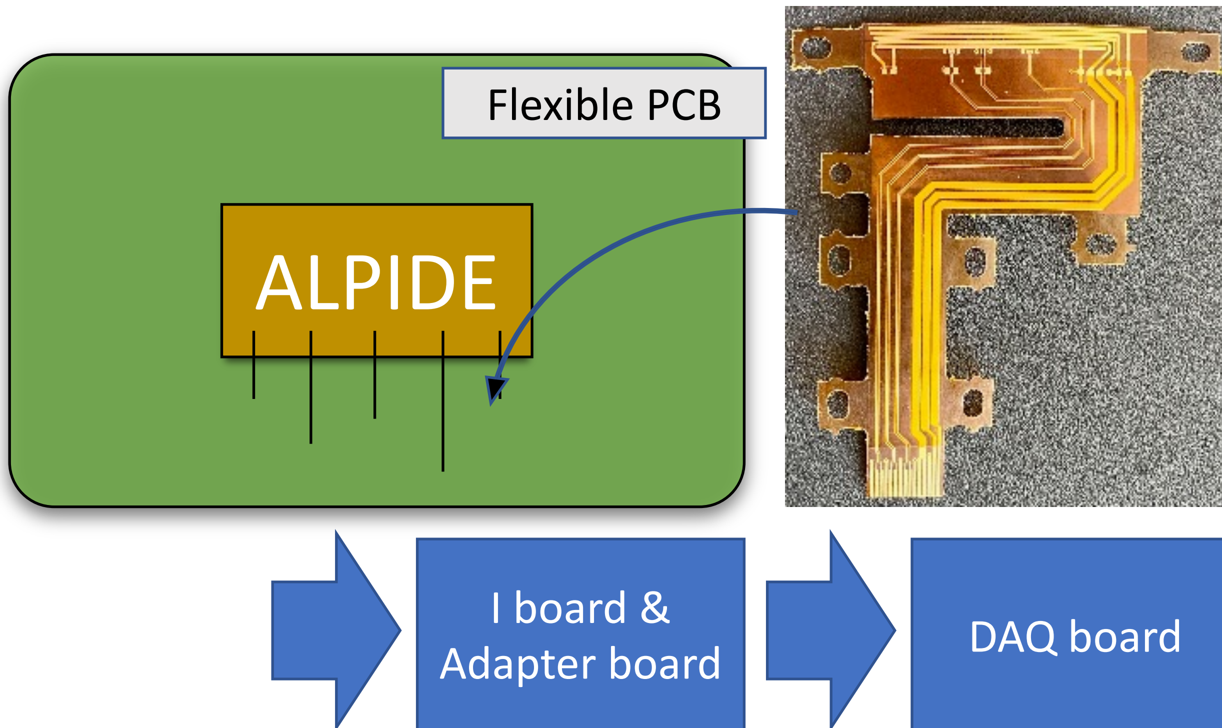


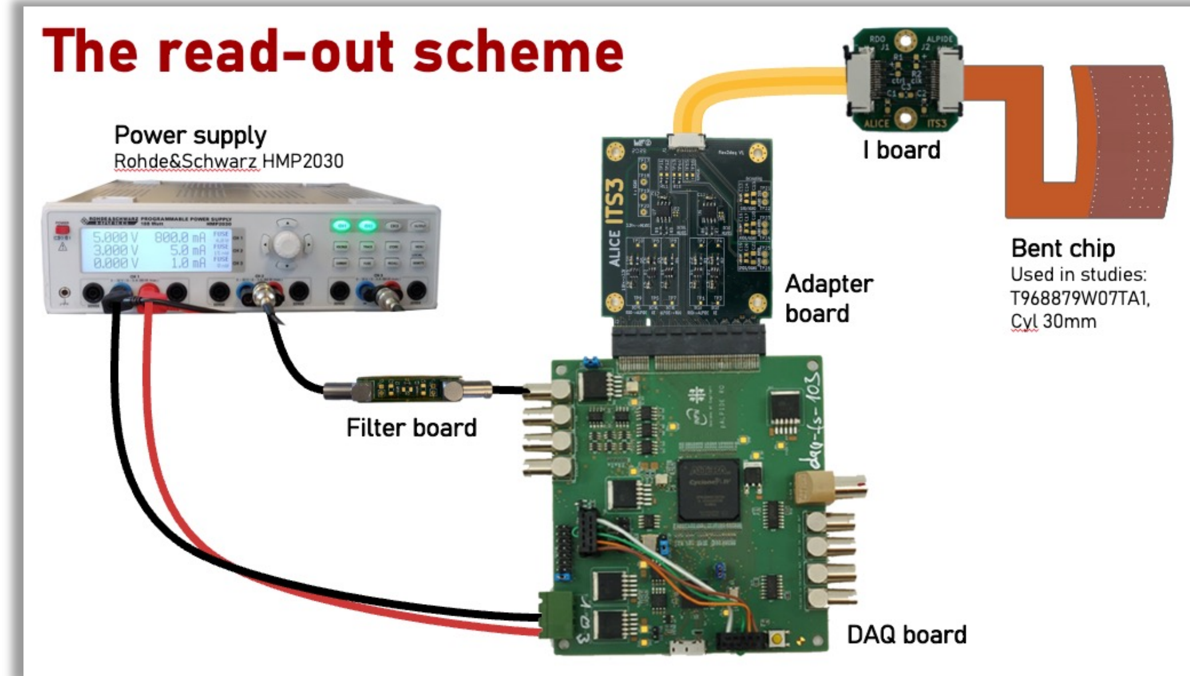


MEMSPACK company wire bonding

Bending test with ALPIDE

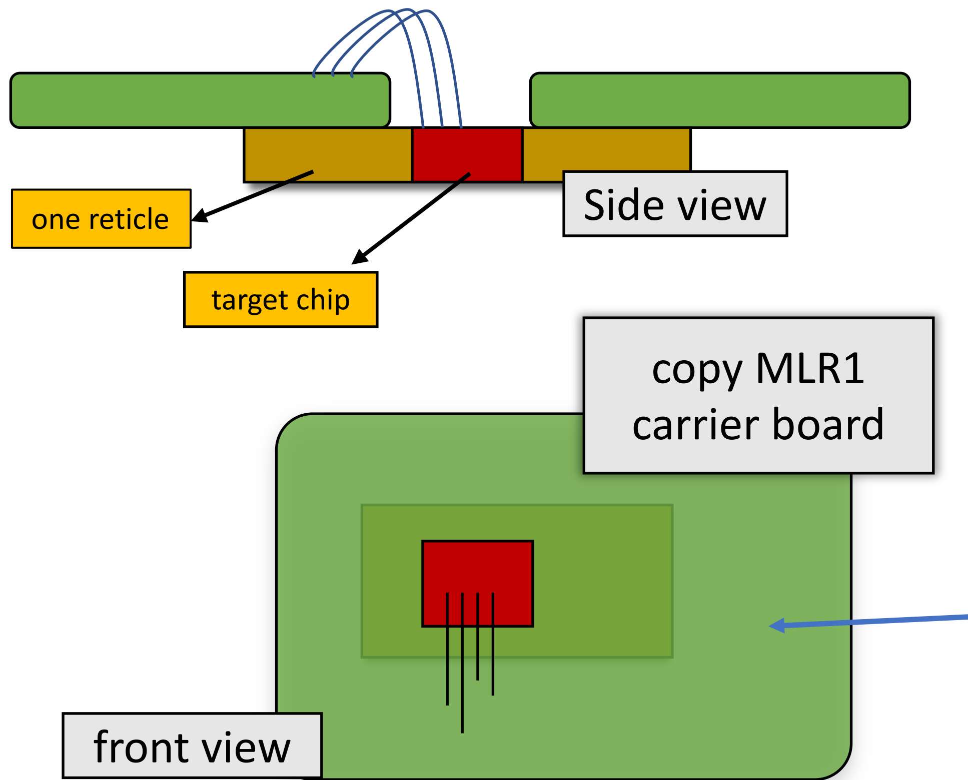
- making the same outlines in our thin PCB like the existing FPC for bent-ALPIDE

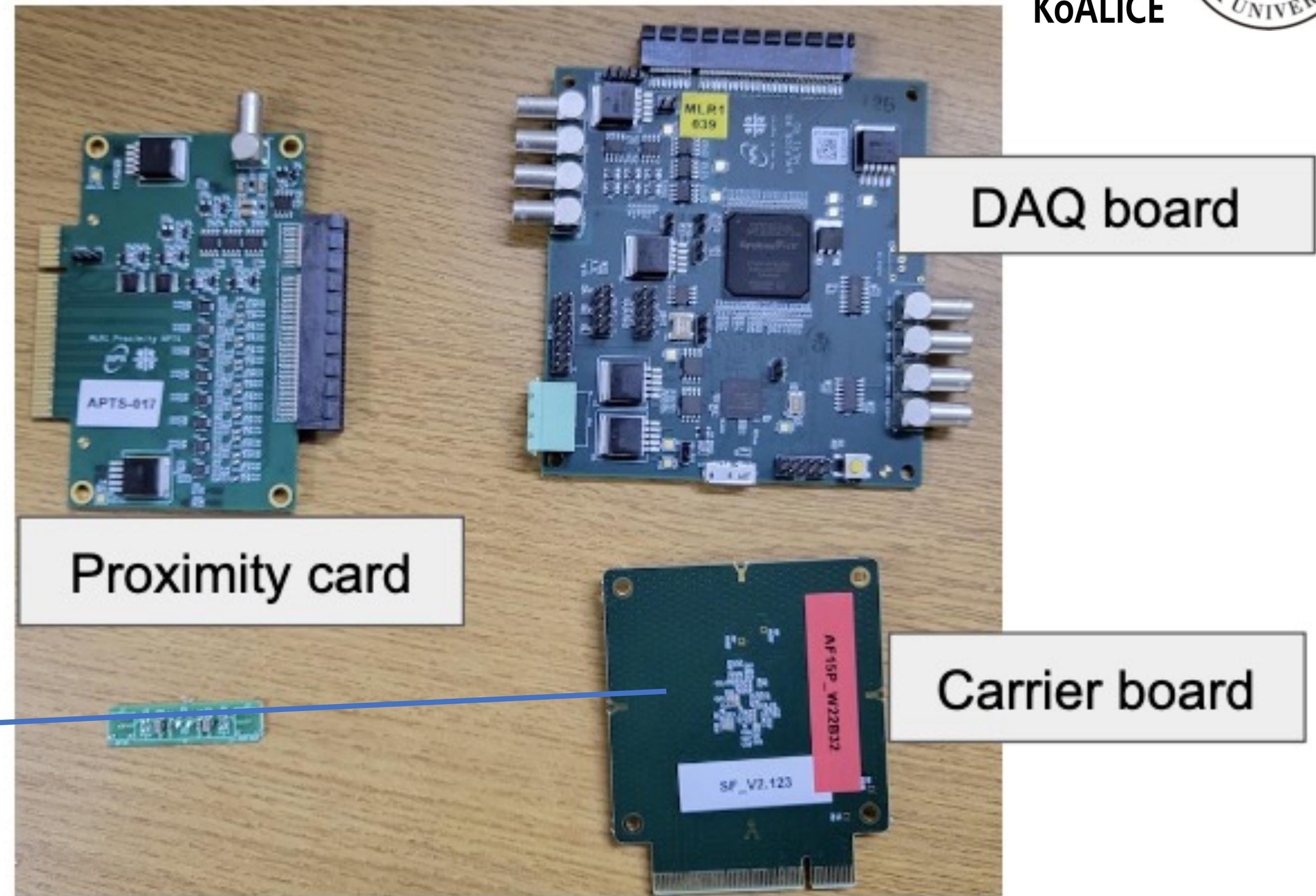


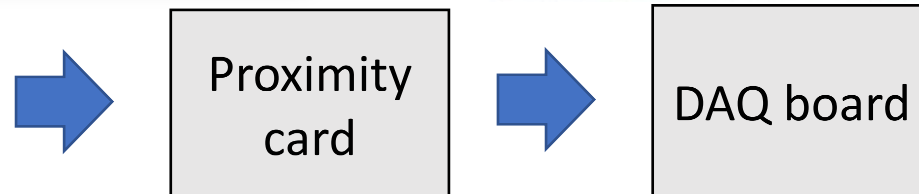


https://indico.cern.ch/event/1053881/contributions/4430248/attachments/2272692/3860104/Investigating_noise_mitigation_strategies_for_bent_ALPIDEs.pdf

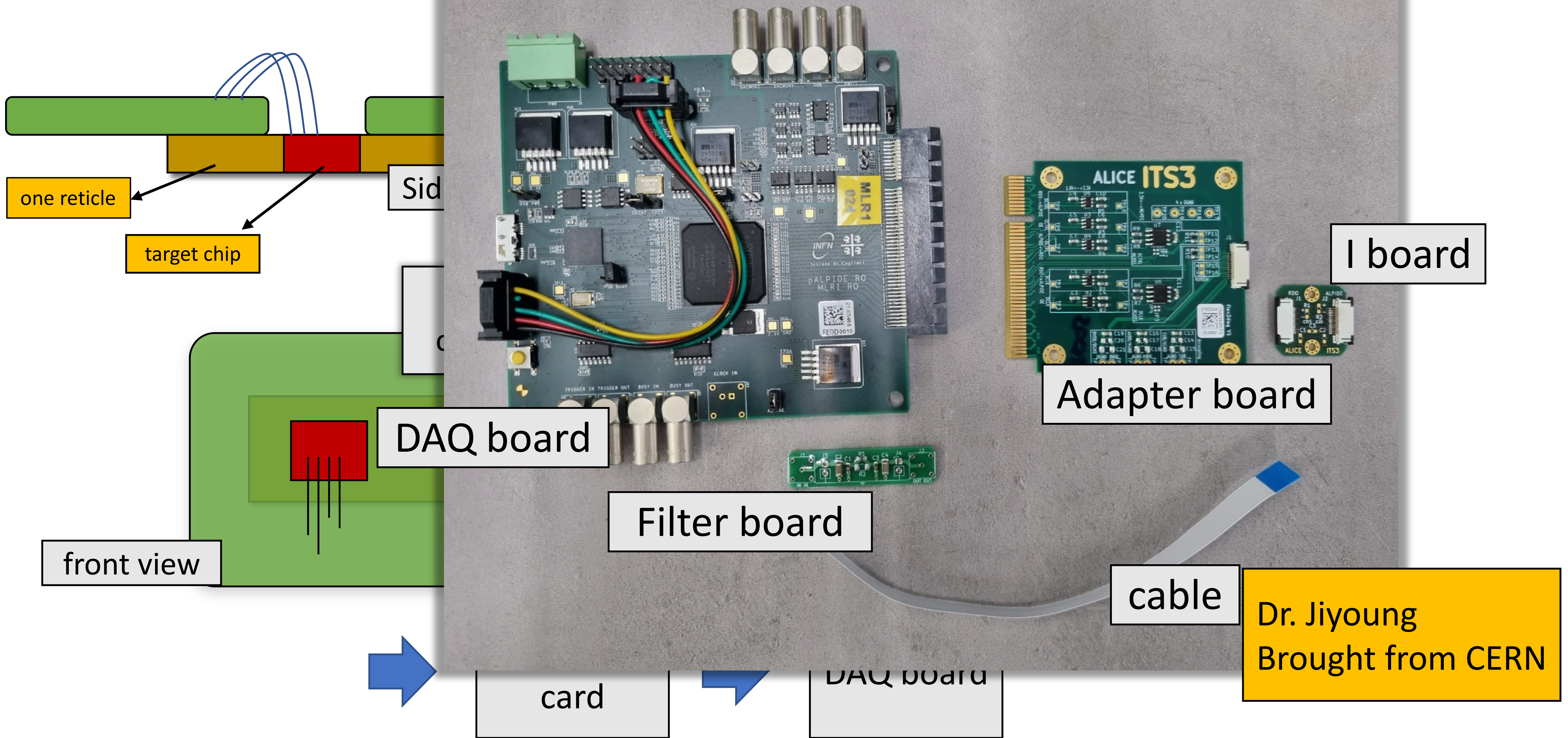
Bending test with MLR1 chip





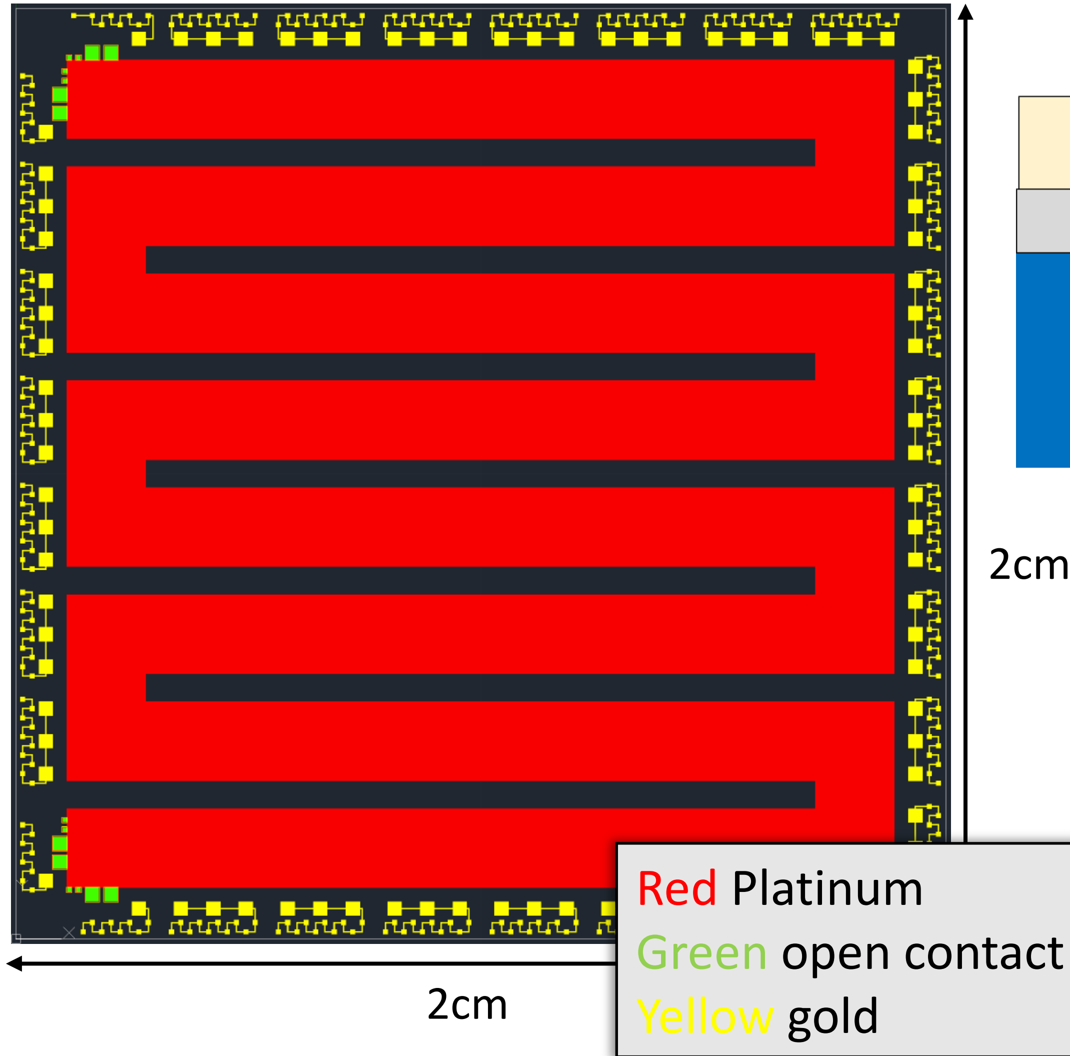


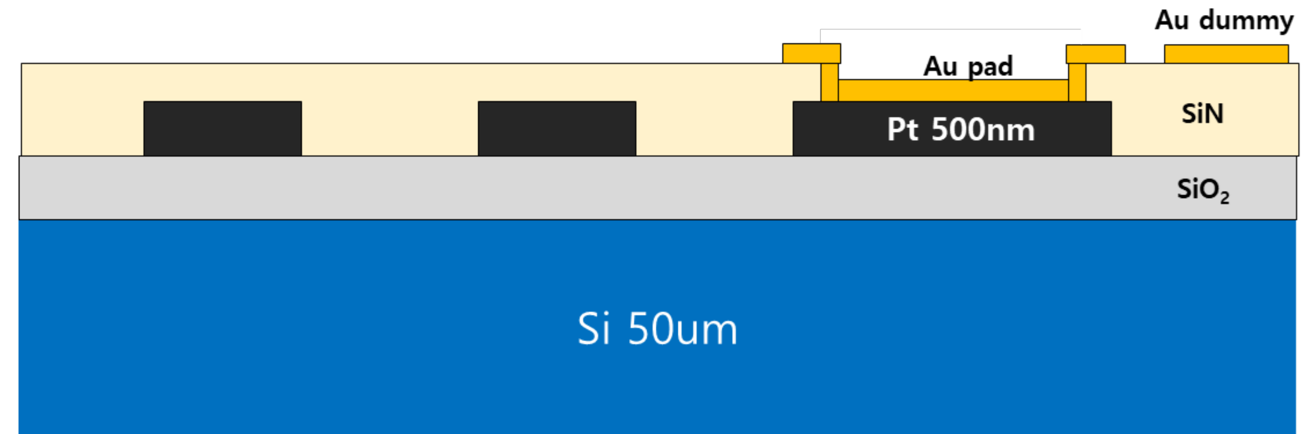
Bending test with MLR1 chip



Dr. Jiyoung
Brought from CERN

Dummy wafer fabrication





Cross sectional view

- Cooling system test of power of 20 mW/cm^2
  - require to Resistance ~ 18 Ω
- Heater line size : 0.5 um x 1.7 mm x 145 mm
- Floor plan for microheater using AutoCAD program
- Gold dummy pads will be used for bonding tests

Summary & outlook

- We are producing the silicon PiN sensor (fabricated in ETRI)
- Test system should be established for fabricated chips.
- Production of FPCB for ALPIDE and MLR1 chip test
- Characterization(threshold, power consumption, stability, etc.) measurement with bent chips
- Dummy wafer production : ALPIDE-size, MLR1-size, heater line
- In the future, the chip temperature is measured inside the chip

Thank you!